Amplifier 02AC198A

Service
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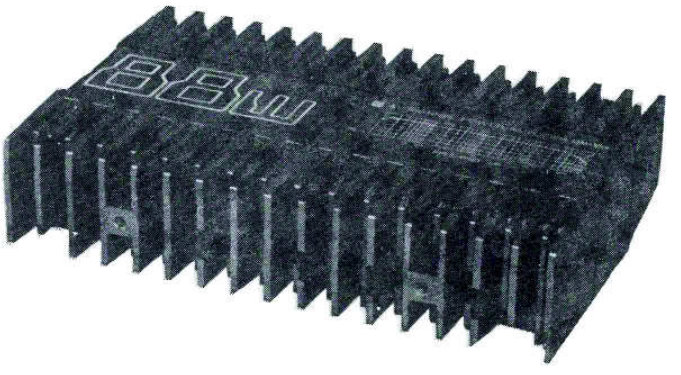


Service Manual

12 V

SPECIFICATIONS

INPUT VOLTAGE	100 mV
INPUT IMPEDANCE	9k OHMS (4 CHANNELS)
POWER OUTPUT	12 WATTS PER CHANNEL (APPROXIMATE)
SPEAKER IMPEDANCE	4 OHMS PER CHANNEL
POWER INPUT	12 VOLTS, NEGATIVE TO EARTH
CURRENT	8 AMPS (MAXIMUM)
SEMI-CONDUCTORS	4 I.C.s 2 DIODES

PHILIPS

Subject to modification
4802 725 17086

PHILIPS

SCHEMATIC

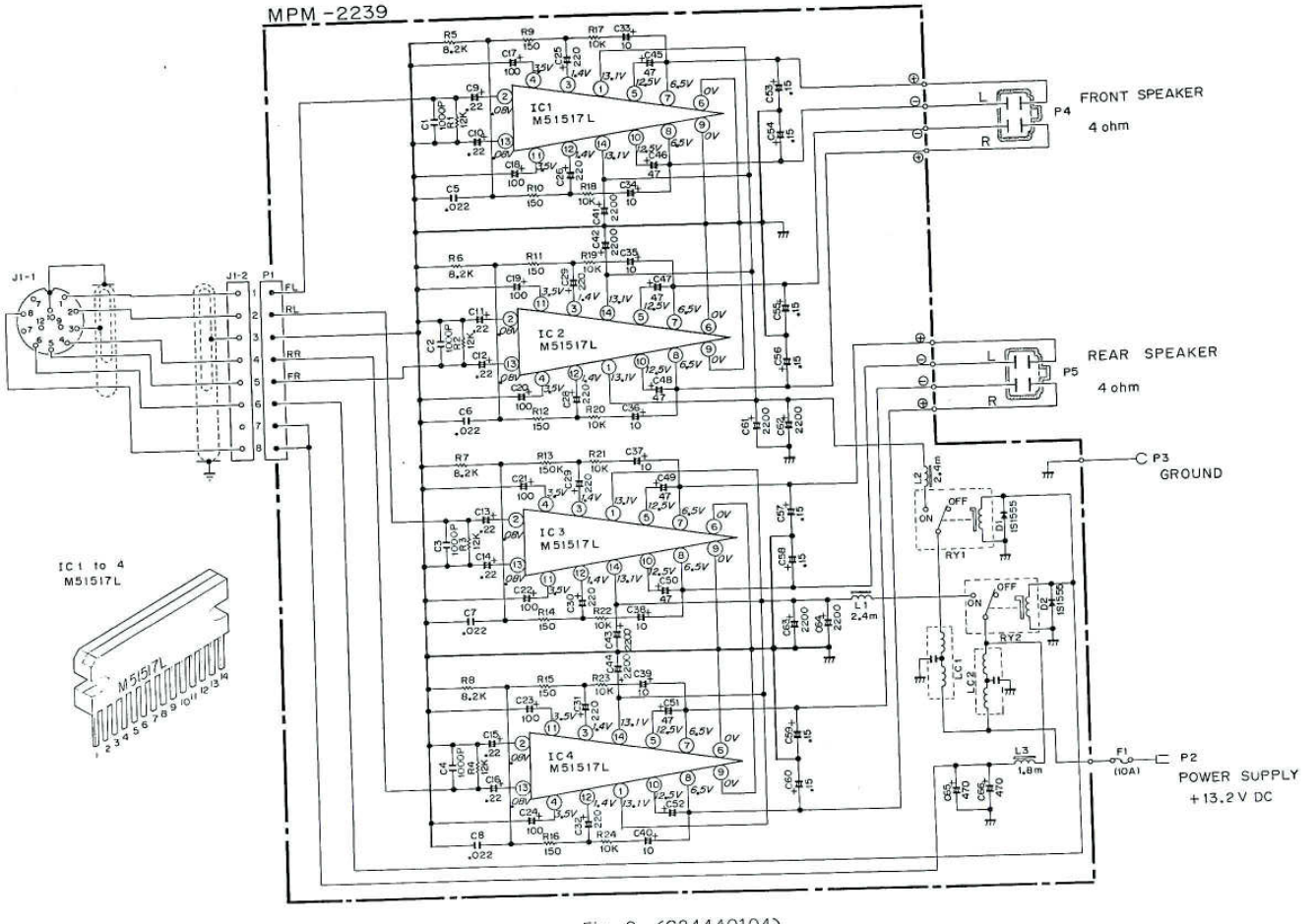


Fig. 3 (C24440104)

NOTES :
1. All capacitance in farad, $\mu=10^{-6}$, $P=10^{-12}$
2. All resistance in ohm, $K=10^{3}$, $M=10^{6}$
3. All inductance in **henry**, $m=10^{-3}$, $\mu=10^{-6}$
4. DC voltages against the chassis measured with 100k ohm/volt meter, power supply set at +13.2 VDC no signal input.

HOOK-UP

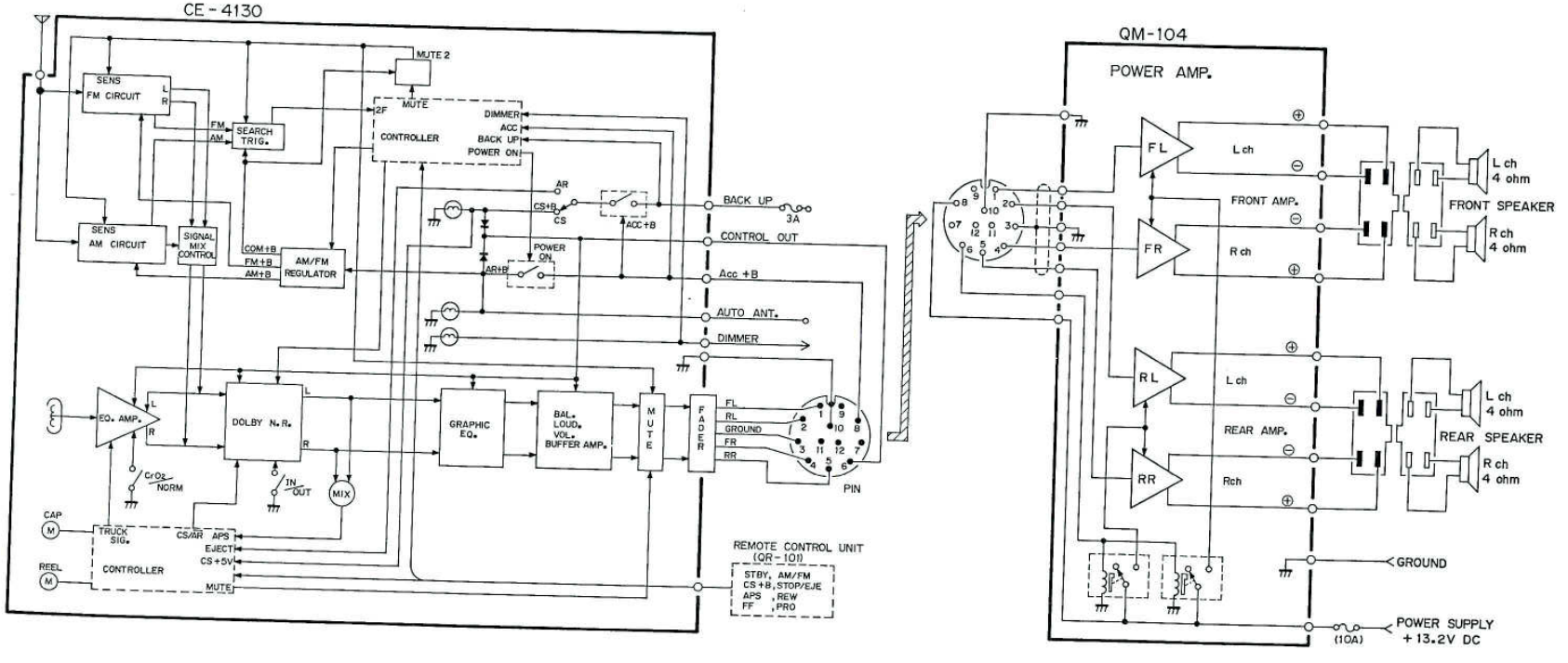


Fig. 2 (C32440104)

REPLACEMENT PARTS LIST

CAPACITORS			
C1-4	1000pF	50V ceramic	4822 122 30027
C17-24	100μF	10V electro	4802 124 47002
C25-32	220μF	10V electro	4802 124 47006
C33-40	10μF	16V electro	4802 124 47044
C41-44	2200μ	16V electro	4802 124 47007
C61-64	2200μF	16V electro	4802 124 47007
C45-52	47μF	16V electro	4802 124 47035

SEMI-CONDUCTORS		
IC1-4	I.C. M51517L	4802 209 87493
D1-2	Diode IS1885	4802 130 37036
MISCELLANEOUS ELECTRICAL		
L1-2	Choke. Filter 2.4mH	4802 152 27049
L3	Choke. Filter 1.8mH	4802 152 27051
J1-2	Wiring sub assy.	4802 321 27237
RY1-2	Relay	4802 281 37005

CONNECTIONS

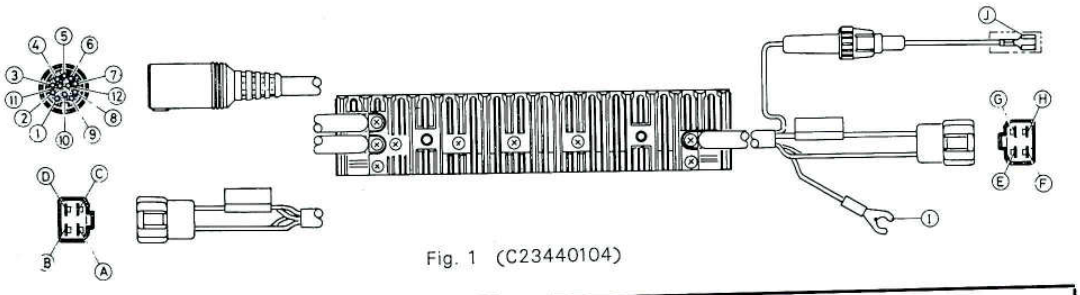


Fig. 1 (C23440104)

A	Front speaker Rch (+)
B	Front speaker Rch (−)
C	Front speaker Lch (+)
D	Front speaker Lch (−)
E	Rear speaker Lch (+)
F	Rear speaker Lch (−)
G	Rear speaker Rch (+)
H	Rear speaker Rch (−)
I	Ground
J	Power supply +13.2 VDC

1	Rear audio signal input L ch
2	Front audio signal input L ch
3	Ground
4	Front audio signal input R ch
5	Rear audio signal input R ch
6	Power supply, amplifier control (ON/OFF)
7	NC
8	Power supply input +13.2 VDC
9	NC
10	Ground
11	NC
12	NC

During the first half cycle ($t_0 \sim t_2$) of the input signal "ei", the potential at point A reaches a maximum of Vc, whille the potential at point A' reaches a minimum of O (ground potential).

Hence, the potential difference across RL (i.e. the voltage applied to RL) varies from O to Vc.

The current during this half cycle is "ic", flows from A to A'.

During the latter half cycle ($t_2 \sim t_4$), the voltage applied across RL again varies from O to Vc, but the current "ic" flows in the opposite direction. If "ic" is assumed to be positive, "ic" will be minus, and the voltage variation be between O and -Vc. Consequently, whereas the voltage change across the RL terminals during a full "ei" cycle is only $O \sim \pm Vc/2$ in the SEPP circuit, the similar changes in the BTL circuit are twice as large ($O \sim \pm Vc$).

The maximum output power pob is expressed by the following formula :-

$$\text{Max. output power } P_{OB} = \frac{\text{Effective voltage } E_B^2}{\text{Load resistance RL}}$$

$$= \frac{(Vc/\sqrt{2})^2}{RL}$$

$$= \frac{Vc^2}{2RL} \quad \cdots\cdots (2)$$

where $E_B = \frac{Vc}{\sqrt{2}}$

3. RATIO OF BTL OUTPUT POWER TO SEPP OUTPUT POWER

The ratio of the BTL output power, P_{OB} (equation 2) to the SEPP output power, P_{OS} (equation 1) is :-

$$P_{OB} : P_{OS} = \frac{Vc^2}{2RL} = \frac{Vc^2}{8RL}$$

i. e. $\frac{P_{OB}\ Vc^2}{8RL} = \frac{P_{OS}\ Vc^2}{2RL}$

* $\frac{P_{OB}}{4} = P_{OS}$

* $P_{OB} = P_{OS} \times 4$

That is, the BTL circuit is capable of producing 4 times the amount of output power than the SEPP circuit under identical conditions such as power source voltage (Vc) and load resistance (RL).

WIRING ON PC BOARD

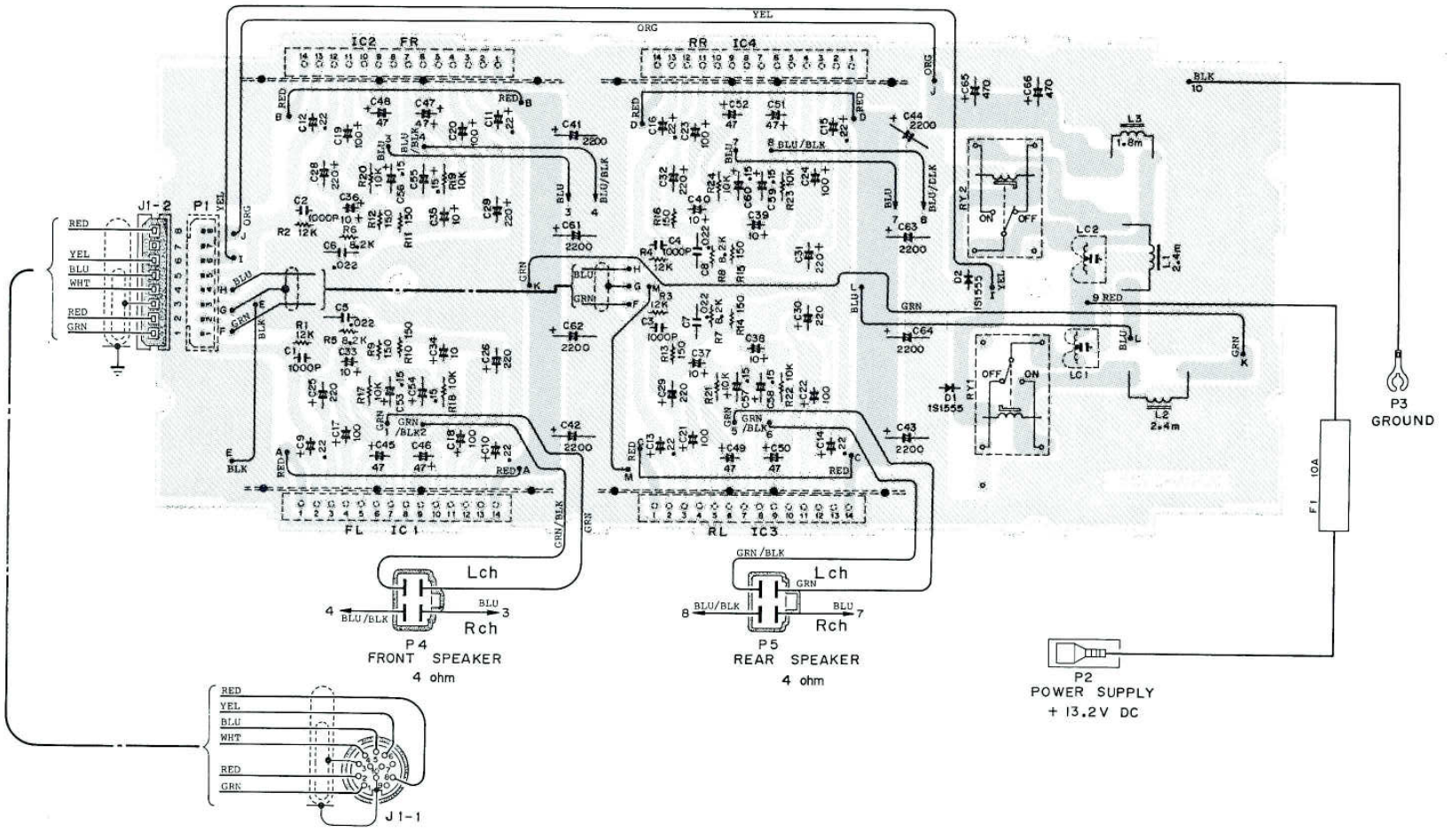


Fig. 4 (C27440104)

Pin No. / IC	1	2	3	4	5	6	7	8	9	10	11	12	13	14
IC 1 to 4	13.1	.08	1.4	3.5	12.5	0	6.5	6.5	0	12.5	3.5	1.4	.08	13.1

(Unit : V)

THE BTL CIRCUIT SYSTEM

1. OPERATING PRINCIPLE

The basic circuit diagram of a **BTL** circuit is shown in Fig. 6 (with resistors and capacitors omitted). Both **AMP 1** and **AMP 2** are composed of identical **SEPP** circuits. The 4 transistors are arranged to form a Wheatstone bridge, with a load resistance (RL) connected between the output terminals (A-A') of both amplifier circuits. An important feature in the **QM-104** is the phase inverter circuit inserted in the circuit for **AMP 2**.

When an input signal "ei" is applied to the input terminals, it is applied unchanged to the **AMP 1** input, but is first inverted by 180° (i.e. becomes "-ei") before being applied to **AMP 2**.

Consequently, during a full swing of the first half of the cycle (shaded portion), the potential at point **A** (AMP 1) will increase to the maximum Vc (voltage of power source) via **Q1** (collector–emitter) (**Q2** is turned OFF), but the potential at point **A'** (AMP 2) will decrease to a minimum of OV (ground potential) via **Q4** (collector – emitter) (**Q3** is turned OFF). Therefore, the potential difference between the two ends of **RL** will be the sum of the 2 voltage changes applied to **A** and **A'**.

The output current "ic" flowing during this period from +VC → **Q1** (collector) → **Q1** (emitter) → **RL** → **Q4** (emitter) → **Q4** (collector) → 0 (ground).

In the same manner, **Q2** and **Q3** are turned ON, and **Q1** and **Q4** turned OFF during the latter half of the ei cycle.

The output current "ic" then flows from +VC → **Q3** (collector) → **Q3** (emitter) → **RL** → **Q2** (emitter) → **Q2** (collector) → 0 (ground).

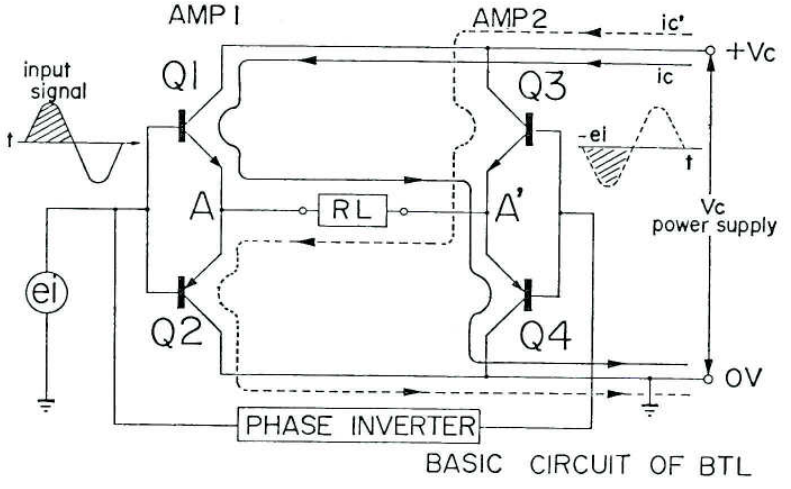


Fig. 6

2. COMPARISON BETWEEN SEPP AND BTL CIRCUITS

2-1. SEPP CIRCUIT OUTPUT POWER

Fig. 7 shows how a single SEPP circuit (for example, AMP 1 in Fig. 6 above) operates.

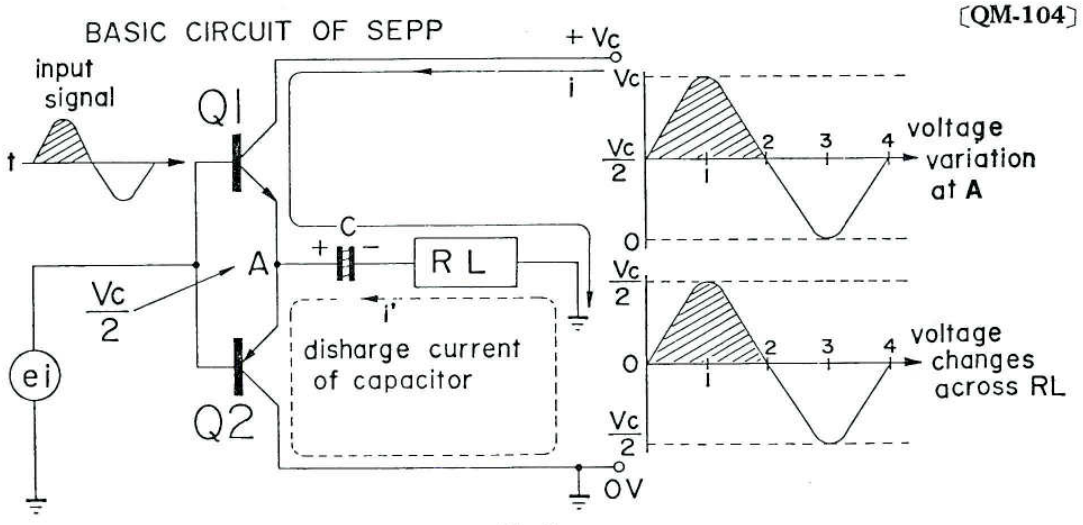


Fig. 7

When the input signal "ei" is applied, the potential at point A varies between a maximum of Vc and a minimum of 0 (ground potential) with a central value of Vc/2. But since direct current is blocked by capacitor C, the potential difference across both ends of RL will vary between a maximum of Vc/2 and a minimum of -Vc/2, centering around O. (This is assuming full swing transistors, and negligible circuit loss).

Since output power is determined by the load resistance RL, and the effective voltage Es applied to RL, the maximum output power Pos available under these conditions may be expressed as follows: (Assuming negligible circuit loss)

$$\text{Max. output power Pos} = \frac{\text{Effective voltage } Es^2}{\text{Load resistance RL}}$$

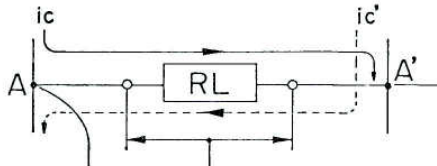
$$\text{Since } Es = \frac{Vc/2}{\sqrt{2}} = \frac{Vc}{2\sqrt{2}}$$

$$Pos = \frac{(Vc/2\sqrt{2})^2}{RL} = \frac{Vc^2}{8RL} \quad \cdots\cdots (1)$$

In other words, $Vs^2/8RL$ is the theoretical SEPP output power.

2-2 BTL CIRCUIT OUTPUT POWER

Fig. 8 indicates the voltage changes ocurring across the load resistance (RL) (between A and A') in the BTL circuit shown in Fig. 6.



ic: CURRENT DURING THE FIRST HALF CYCLE (to - t2) OF INPUT SIGNAL ei

ic': CURRENT DURING THE LATTER HALF CYCLE (t2 - t4) OF INPUT SIGNAL ei

INPUT SIGNAL	TIME	POTENTIAL AT POINT A	POTENTIAL AT POINT A'	POTENTIAL DIFFERENCE BETWEEN A & A'	VOLTAGE ACROSS RL	CURRENT
-ei 0 ei	t o	Vc/2	Vc/2	0	-Vc 0 Vc	
	t 1	Vc	0	Vc		
	t 2	Vc/2	Vc/2	0		
	t 3	0	Vc	Vc (-Vc)		
	t 4	Vc/2	Vc/2	0		

Fig. 8