AWA THORN

The new Colour Television Chassis 4KA Series

INTRODUCTION

The colour receivers being produced by AWA-Thorn Consumer Products use an all solid-state chassis known as the 4KA. The design of this chassis is based on the 4000 series chassis developed in England by T.C.E. (Thorn Consumer Electronics). The 4KA differs from the 4000 series chassis mainly in the following areas.

	AWA-THORN 4KA	T.C.E. 4000 UK Version	T.C.E. 4000 Export Version
Tuner	Rotary turret	Varactor Diode UHF	Varactor Diode VHF/UHF
Video I.F. (MHz)	36.875	39.4	38.9
Sound I.F. (MHz)	5.5	6.0	5.5
Mains Isolated chassis	Yes	No	No

a) Tuner

The 4KA chassis uses a rotary turret tuner with pre-set fine-tuning in place of the varactor diode tuner of the 4000.

b) Video I.F. Amplifier

The recommended Australian video I.F. carrier frequency of 36.875MHz is used in the 4KA, whilst the 4000 chassis operates at the CCIR standard frequencies. These are 39.4MHz for receivers intended for the U.K. market and 38.9MHz for sets for sale in Europe.

c) Sound I.F. Amplifier

The sound carrier in the U.K. standards has 6MHz separation from the video carrier, compared with the 5.5MHz intercarrier frequency of the Australian system.

d) Power Supply

In the 4KA chassis a fully isolated mains transformer is employed, allowing the chassis to be earthed as is customary with existing Australian monochrome receivers. The 4000 chassis is a "hot" chassis. The main H.T. is derived directly from the mains supply by means of a bridge rectifier. This results in the chassis being at half the mains supply voltage irrespective of the polarity of the mains connection.

In addition to these major differences there are a number of minor circuit changes, made to optimise performance for Australian conditions. There are also changes to allow the use of locally sourced components.

The 4000 chassis (and 4KA) has a number of novel features, both electrical and mechanical. Advantage is taken of new technology and this results in a chassis with outstanding performance and reliability. At the same time the intelligent use of the module principle allows rapid and easy service, both in the home and the workshop.

When the 4000 chassis was introduced a manual was released giving a full technical description. In the sections to follow, the material of the 4000 series chassis manual is reproduced in its entirety. Where the Australian made 4KA chassis differs, supplementary sections have been added which describes the differences in detail. Some of the features of the 4000 chassis such as touch tuning will not be available in the initial versions of the 4KA. The description of these features has been retained, however, it being felt that the information will prove both interesting and educational to technical people in this country. In addition it can not be too far in the future that colour television receivers in Australia will be equipped with such facilities.

SECTION 2
Mechanical Construction

(Refer to pages 6 & 7 for details)

Comments on 4KA differences

The main differences of mechanical construction of the 4KA compared with the 4000 are brought about by the use of a rotary turret tuner and a mains isolating power transformer. The Tuner Drawer Unit referred to in section 2a and 2g and shown at the left in Fig. 2.1 is not present with the 4KA chassis. The varactor diode tuner shown mounted on the signal board in Fig. 2.3 is also omitted. The turret tuner used instead is mounted to the front control panel together with the mains switch and slider potentiometers provided as customer controls. The 4KA power transformer mounts to the cabinet base on the left-hand side (seen from the back). Connections from it to the chassis proper are made by pluggable connections incorporated in the main cableform. The small transformer referred to in section 2b is not present in the 4KA, its functions being carried out by this power transformer.

SECTION 3
Comment on 4KA Circuitry differences

(Refer to pages 9-2 for details)

The 4KA chassis uses a power transformer which isolates the chassis from the mains supply. The primary is provided with taps to accept nominal mains voltages of 240V and 250V. The receiver will operate satisfactorily with voltages up to 10% above or below the nominal.

The 3 secondary windings supply voltages for the following are:

a) Input to bridge rectifier for main H.T. (+165V). This winding also supplies the automative degaussing circuit.
b) Input to bridge rectifier for +13V supply for switched mode driver transistor.
c) Heaters of colour picture tube.

Note

The 4000 circuit description refers to the mains H.T. supply voltage of 155V. Late changes have resulted in the voltage being increased to 165V. This voltage applies to the 4KA chassis also.

In section 3e, second paragraph, reference is made to the use of IC151 to obtain a 33V supply. This is required in the 4000 chassis to feed the variable capacity diodes in the tuner unit. It is not necessary in the 4KA.

SECTION 4
Comment on 4KA Circuit differences

(Refer to pages 13-17 for details)

The turret tuner of the 4KA chassis is similar in mechanical and electrical characteristics to that presently used in solid-state monochrome receivers. Special attention is paid to obtaining optimum performance with respect to frequency and phase response over the received channel. The region around the colour carrier frequency is more critical in reception of colour than is the case with monochrome signals.

Interconnections between tuner and the main chassis are via plug and socket and are fewer than with the 4000 chassis. Apart from the Video I.F. coaxial connection there is only the + 12V H.T. supply and the RF AGC voltage.

Note

The tuner described in section 4a is a combined VHF/UHF unit, the export version of the 4000 intended for use in Europe where colour 625 line transmissions are on both VHF and UHF. In the U.K. only UHF bands are utilised for the 625 line service.

CONTENTS

Section 1. NEW TECHNOLOGY IN THE 4000 SERIES

a. The 110° Colour Tube

The most significant change from previous Thorn colour chassis designs is the introduction of the 110°, 29 mm diameter neck, cathode ray tube. This tube, used with precision toroidal scan coils has enabled a standard of convergence uniformity to be obtained which would not have been considered possible when 110° tubes were first introduced. However, the increased scanning angle almost doubles the energy required for horizontal deflection and increases the power dissipated in the vertical coils by a factor of four. The addition of north-south and east-west pin-cushion correction circuits are, therefore, essential requirements.

These factors have led to an entirely new chassis concept making full use of the latest semiconductor and thick-film technologies.

b. Semiconductor Devices

The Thorn 4000 series chassis incorporates nine monolithic silicon integrated-circuits of the latest type. Three of these devices have been designed in collaboration with Thorn engineers to meet the specific requirements of the 4000 series.

Six of the nine ICs are used to provide complex signal processing functions, and together they contain approximately 400 transistors and diodes giving an average of over 66 semiconductor functions per chip. Two other ICs are used to provide stabilised voltage rails and in both cases give a performance which could not be obtained economically using discrete components. The remaining IC is a complete audio amplifier system and is capable of giving 4 watts rms continuous output power. The device package incorporates a large finned heatsink.

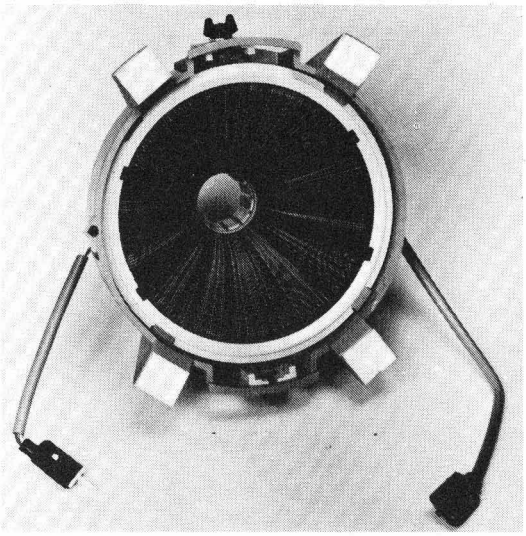


Fig. 1.1

A single power transistor is used to provide the line scanning energy, and is capable of operating at 1500 volts and passing a peak collector current of 5 amps. In the interests of long-term reliability, however, it is not used to the full limits of its capability in the 4000 series design.

c. Thick-Film Circuits

The 4000 series chassis makes full use of the latest developments in thick-film technology by using seven assemblies incorporating active devices; three purpose-built potentiometers; several multiple resistor units, and numerous fixed and variable single-resistor units from standard ranges.

Thick-film circuits are produced by depositing conductors and resistors on a ceramic base or substrate. This material has a thermal conductivity which is similar to that of mild steel and thus forms an excellent heatsink for sections of circuitry with medium- or high-power dissipation. Modern production techniques, using a scanning power laser, permit twenty deposited resistors to be trimmed to 5% tolerance in three seconds. Resistors with tolerances of better than 5% may also be obtained to meet specification requirements.

Further advantage can be obtained by utilising the common substrate for balanced circuit designs so that the effect of thermal drift on component values is arranged to cancel. This technique is used to ensure good stability during warm-up in the 4000 convergence circuits.

Active thick-film circuit assemblies incorporate discrete capacitors and semiconductor devices but are fully encapsulated to protect them from contamination and damage. The assemblies are usually mounted perpendicular to the main printed boards on short connecting leads and may be treated as functional blocks for fault-finding and service replacement purposes. Thick-film potentiometer units, such as the 4000 series focus control, have been designed to operate at up to 9kV and have resistance values of tens of megohms, and still retain excellent stability during use. Thick-film controls are also used to meet other special circuit requirements in the 4000 series. For example, the vertical shift control consists of a number of high wattage resistor elements, each with the appropriate value and rating to give a linear control action, which is selected by a make-before-break non-detent rotary switch.

Section 2. MECHANICAL CONSTRUCTION

Refer to introductory notes on page 3

a. General Construction

The Thorn 4000 series receiver is constructed in modular form and consists of five major assemblies which incorporate the following: The Power Supply; Line Timebase and Switched Mode Supply; The Signals Module; Field Timebase; and CRT Neck Unit. In addition, there are three smaller assemblies comprising: The hand-held Convergence Set-Up Unit; Tuner Drawer Unit, with channel-selection components; and the CRT Base Assembly. The relative size and position of each unit is shown in Fig. 2.1.

A substantial main frame is mounted on runners in the cabinet base which permit withdrawal of the complete chassis assembly to give excellent access to the print-side of signal and power module boards. Also full access to the component side of these modules can be obtained by hinging them downwards as shown. All modules are easily detachable from the main frame for servicing.

The same basic modules are used for all receiver model sizes. These are fitted to a standard size main frame and associated cableform,except for Model 3C03 with a 20" diagonal picture tube which utilises a smaller version of the main frame and cableform to suit the more compact cabinet.

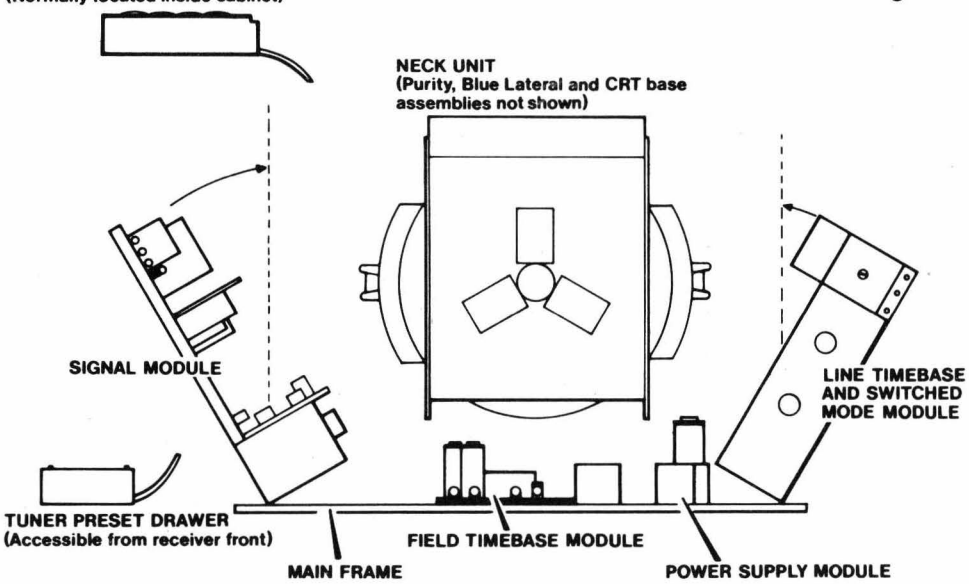
b. Power Supply

This contains a small transformer to supply the CRT heater and a subsidiary supply for the switched mode drive together with the degauss components.

c. Line Timebase and Switched Mode

The line timebase and switched mode supply module accommodates the switched mode supply circuits, sync and line oscillator sections, line output circuit, and EHT generator and focus systems. A plan view of the unit with the major components and preset controls identified is shown in Fig. 2.2. The module is totally plug-and-socket connected to other sections of the receiver, and can be quickly detached from the main frame for servicing. Servicing is also made easier due to the fact that power transistors VT301, VT305, VT307 and IC301 are all mounted in sockets. Preset controls on the circuit board are accessible from the print-side for easy adjustment. The switched-mode auto-transformer and EHT transformers are cooled by a large finned heatsink which is mounted across the top on the module to the rear of the power and EHT sections as indicated in Fig. 2.2.

Fig. 2.1



d. Signal Module

This module carries the varicap tuner; IF and demodulator circuits; sound intercarrier IF demodulator and output ICs; decoder and video output circuits; and secondary power supply and stabilisation systems. A plan view of the module with major assemblies and preset adjustments identified is shown in Fig. 2.3. The module may be easily detached from the main frame and completely disconnected by removal of plugs and sockets. Individual components or assemblies on the module which are replaceable without soldering include all three decoder integrated circuits IC155, IC156, IC157; the sound output IC153 complete with heatsink; the IF panel, which includes IC101 the colour processing panel; and the varicap tuner unit.

e. Field Timebase Module

The field timebase module which is shown in Fig. 2.4, incorporates a thick-film vertical oscillator circuit with N–S pincushion correction; a thick-film amplifier driver section and two complementary power output transistors mounted on a large finned heatsink. In addition, there is a circuit which generates CRT blanking pulses and a purpose-designed thick-film potentiometer system to provide vertical picture shift. All adjustable controls are accessible from the receiver back and the module can be easily detached and unplugged for service replacement.

f. Tube Neck Unit

This unit is constructed around a precision deflection toroid assembly and includes thick-film convergence drive and matrix components; convergence power output transistors, mounted on large area heatsinks; convergence and lateral coils with purity rings; and a line-shaper board which houses 'S' correction, linearity and shift components. Fig. 2.5 shows the module, as viewed from the CRT base after removal of the lateral and purity assemblies. Connections to other sections are carried via a floating edge-connector so that modules can easily be replaced in the field if necessary.

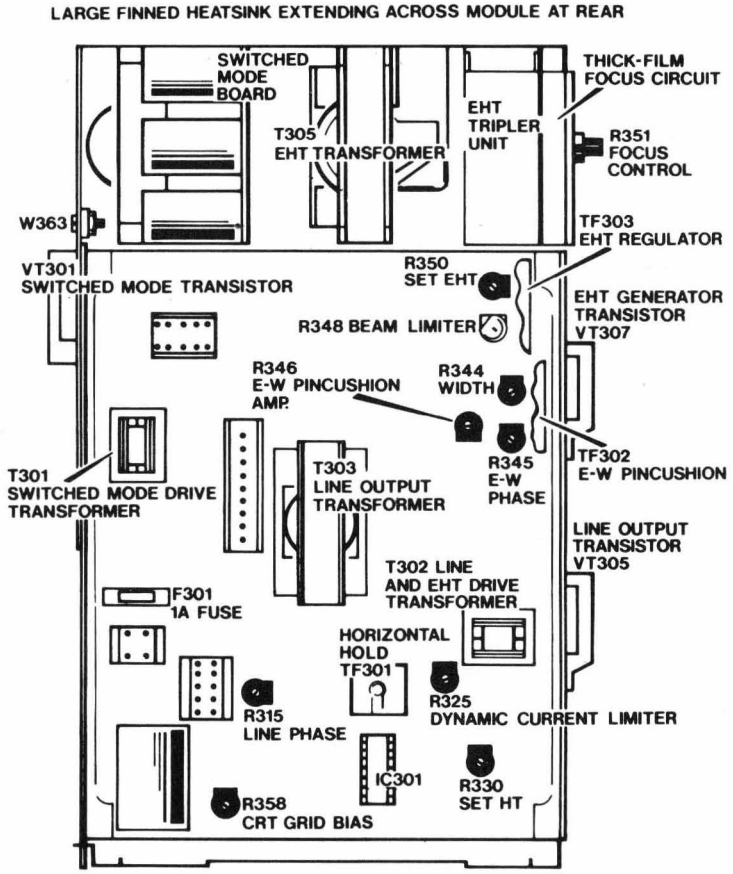


Fig. 2.2

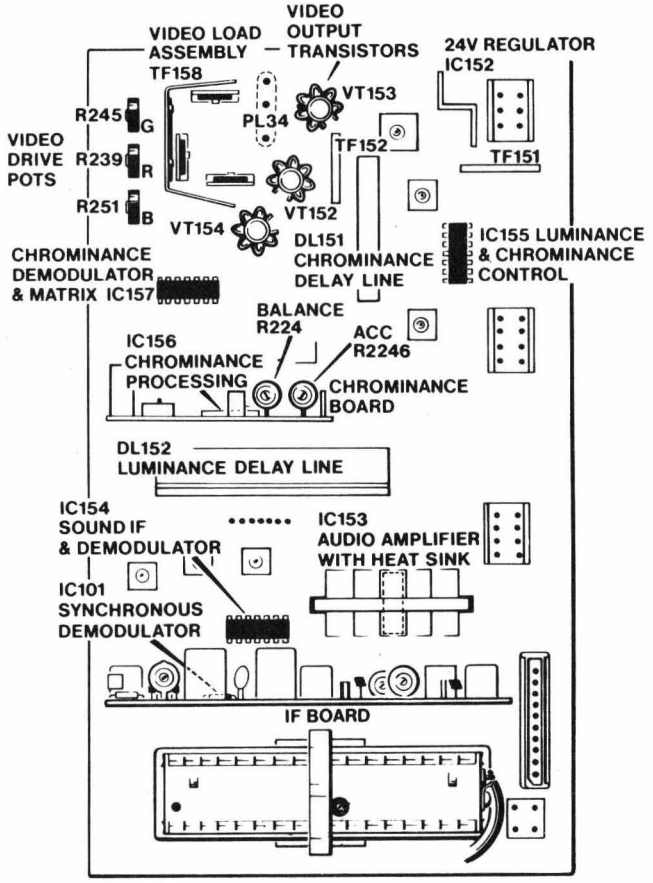


Fig. 2.3

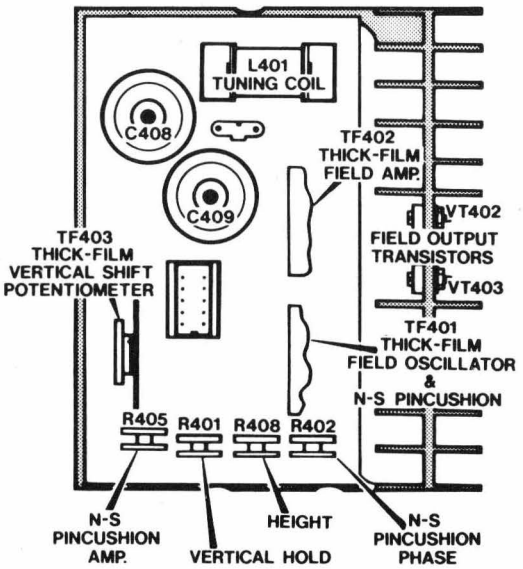
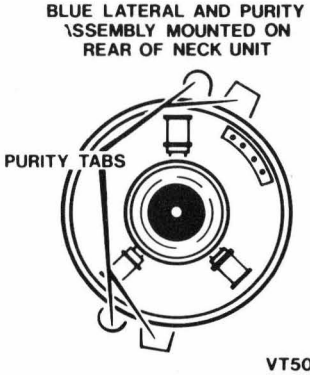


Fig. 2.4



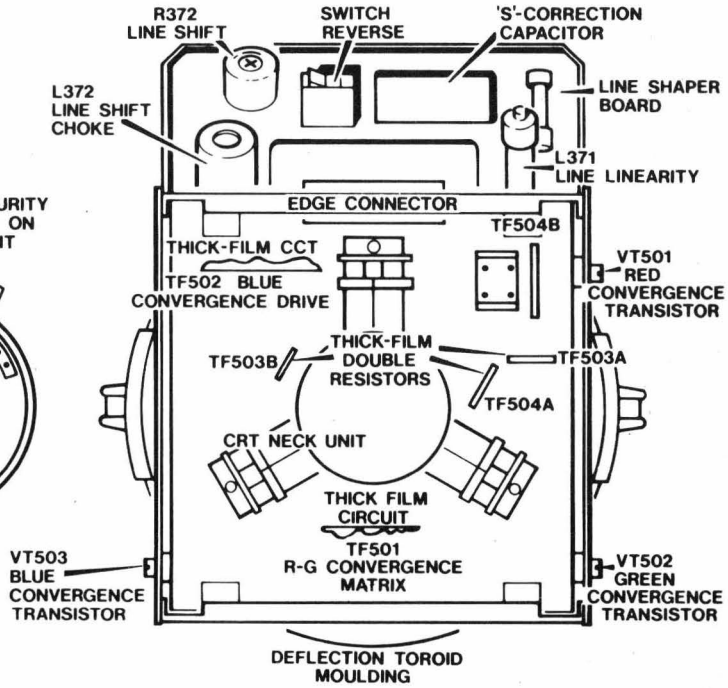


Fig. 2.5

g. Tuning Drawer, Hand-Held Unit, and User Controls

The drawer unit located at the front of the cabinet, contains a small printed board carrying tuning potentiometers plus their associated circuitry including band-change switching, and an AFC interface network. A separate tuning knob and indicator dial is provided for each touch-tune selection pad. Although user control assemblies vary with presentation all are of the slider type. Neon lamps switched by transistors are provided to indicate the channel selected. The hand-held unit is basically a small plastics box which is housed adjacent to the signal module except when convergence set-up is required. It can then be withdrawn completely from the cabinet to the extent of its cableform to facilitate adjustments from the front of the receiver. Thumb-wheel potentiometers give twelve different dynamic convergence corrections and there are four static controls which enable centre convergence to be optimised without adjustment of the magnets on the CRT neck. A gun switch is incorporated to remove the blue display whilst converging red and green. The CRT base assembly includes spark-gaps and decoupling components to protect the receiver from damage due to CRT flashover. Each gun has an A1 voltage potentiometer and associated cut-off switch which may be used to obtain accurate grey-scale adjustment.

Section 3. MEDIUM- AND LOW-VOLTAGE POWER SUPPLIES Refer to introductory notes on page 3

a. Mains Derived Supplies

The main power supply system in the Thorn 4000 series design is of the high-frequency switched mode type and a full description of the circuit is given later. The switched mode circuit requires a high current; high voltage DC feed; and a low voltage supply for the driving circuits, which must be mains derived to enable the circuit to start up after switch on. A circuit of the three supply systems which directly derive their energy from the AC mains input is given in Fig. 3.1.

The transformer T801 has primary tappings to accept nominal mains inputs of 200V, 220V and 240V. Selection of the appropriate tap will permit the receiver to operate over the range 180V to 265V. The thermal trip is to protect the transformer against damage due to continuous overloading and if triggered will automatically reset after approximately 15 minutes.

Full mains input voltage is fed via a bridge rectifier W801 and its associated circuit and a surge limiting resistor R801 Reservoir capacitor C802 is thus charged to a potential which is determined by the mains input and can vary between 230V and 350V DC. This voltage, which is negative with respect to chassis, is fed to the switched mode power supply section via limiting resistor R804, 1A fuse F301 and choke L301. The use of a bridge rectifier results in the chassis always being at half-mains voltage and this must be borne in mind during servicing, etc.

The second mains-derived DC supply shown in Fig. 3.1 is provided by a winding on mains transformer T801 and a bridge rectifier unit W301. Output from reservoir capacitor C305 is positive with respect to chassis and can vary between 40V and 60V over the range of acceptable mains input. This supply is used to feed the switched mode driver transistor and integrated circuit IC301. This device contains an internal stabiliser which holds the voltage across C310 at 13V. The 30V Zener is included to limit dissipation in the IC stabiliser under high input voltage conditions.

The third mains-derived supply shown in Fig. 3.1 is 6.3V AC for the CRT heaters which is obtained from a further isolated winding on T801.

b. Shunt Switched Mode Principles

The main power supply requirements of the 4000 series circuit are 205V at 20W for the video output stages; 155V at 80W for the line output and EHT generator circuits; 32V at 60W for the field timebase, audio output, decoder and signal circuits. All three supplies are developed and stabilised by a single, high efficiency, shunt switched mode circuit.

Fig. 3.2 A and B illustrate the basic principle of shunt switched mode operation. D1 rectifies the mains input and charges C1 making the emitter of the switching transistor 'T' approximately 300V negative with respect to chassis. When 'T' is turned on this voltage appears across 'L' and results in a steadily rising current flowing through 'L' and around the circuit as shown in Fig. 3.2A.

When the switching transistor 'T' is turned off, the magnetic field stored in the core of inductor 'L' starts to collapse and the emf across 'L' reverses direction making the top positive with respect to chassis as shown in Fig. 3.2B. Rectifier diodes D2 and D3 are now forward biased and the falling current in 'L' flows through the diodes charging reservoir capacitors C2 and C3 as shown.

The magnitude of the reverse emf which appears across 'L' after the switching transistor turns off is determined by the amount of current flowing in 'L' at the instant of switch off. If the transistor has been turned on for a relatively long time the current in 'L' will have reached a high value and a large emf and high rectified output voltage will result as shown in Fig. 3.3A. When the on and off periods or mark-to-space ratio of the transistor are approximately equal, the input and output voltages will be similar as shown in Fig. 3.3B. A short 'on' period,

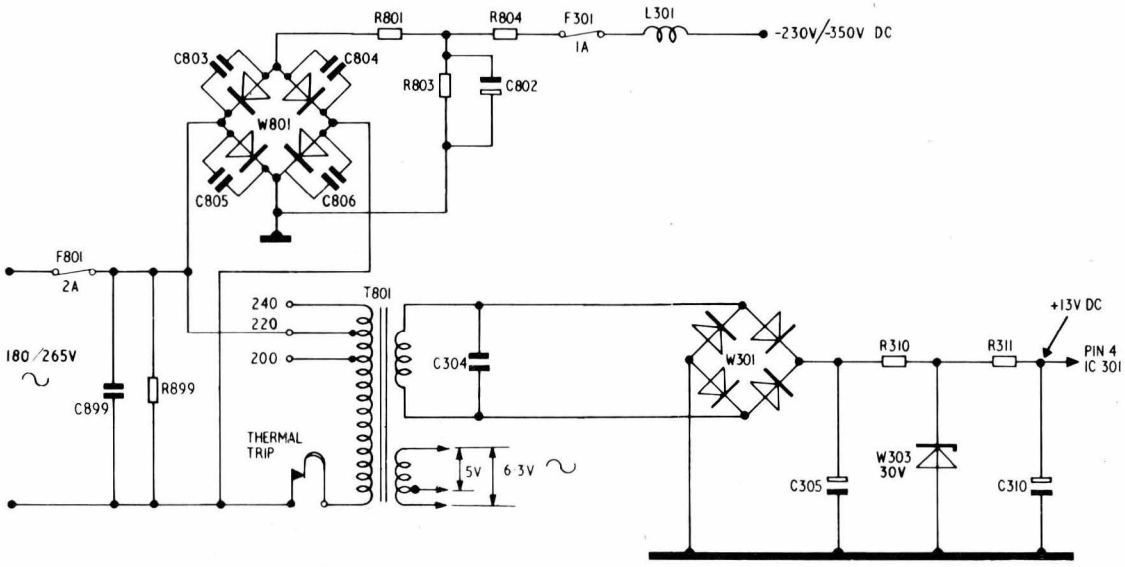


Fig. 3.1

followed by a relatively long 'off' period will produce an output voltage which is lower than the input voltage as indicated in Fig. 3.3C.

The shunt switched mode circuit can therefore be designed to give an output voltage which may be above or below the DC input voltage. Rectifiers fed from tapping points on the main coil will give lower output rail voltages, and an overwind plus rectifier in series with the main supply can be used for higher voltages as shown in Fig. 3.4.

An automatic circuit can be provided to control mark-to-space ratio so that a stabilising action against changes in input voltage and load current is obtained, and a high frequency switching rate may be used so that low frequency ripple voltages are smoothed out.

Switched mode circuits have high efficiency because for most of the time the switching transistor is either saturated with very little voltage drop between emitter and collector, or cut-off. Both conditions give low wattage dissipation and the change and control of voltage levels is thus achieved without attendant problems due to excessive generation of heat.

c. Switched Mode Control Circuit

A circuit of the switched mode control and drive system is given in Fig. 3.4. Switching transistor VT301 is driven via VT302 from an integrated circuit IC301. The IC contains an oscillator locked to the line frequency of 15.625kHz and supplies a falling ramp waveform to a Schmitt trigger mark-to-space control circuit as shown.

The power supply's nominal +155V DC output rail is monitored by zener diode W307 and potential divider R367, R330 and TF305. W307 is a 130V device. As there is a constant 130V drop across W307, any output voltage variations due to loading, input voltage or ripple, will be present with high amplitude at the IC input. R328, C321 and C322 provide a damped time-constant for the control loop.

Three separated cycles of the oscillator output ramp waveform are shown in Fig. 3.4A, B and C with control voltages corresponding to high, correct and low input voltages superimposed. Waveform B shows a correct input voltage indication which results in a nominal 24μs switched mode conduction period. On waveform A a high input voltage is indicated and the switched mode conduction period is terminated earlier. Waveform C shows how a low input indication will extend switched mode conduction thus passing more energy to auto-transformer T361 which will in turn increase the rectified rail voltage output. It should be noted that driver transformer T301 is phased so that the switching transistor VT301 is off when driver transistor VT302 is on, and vice versa. This is to ensure that a low impedance is present across the base and emitter of VT301 when the emitter-collector voltage is at its peak to give maximum reliability.

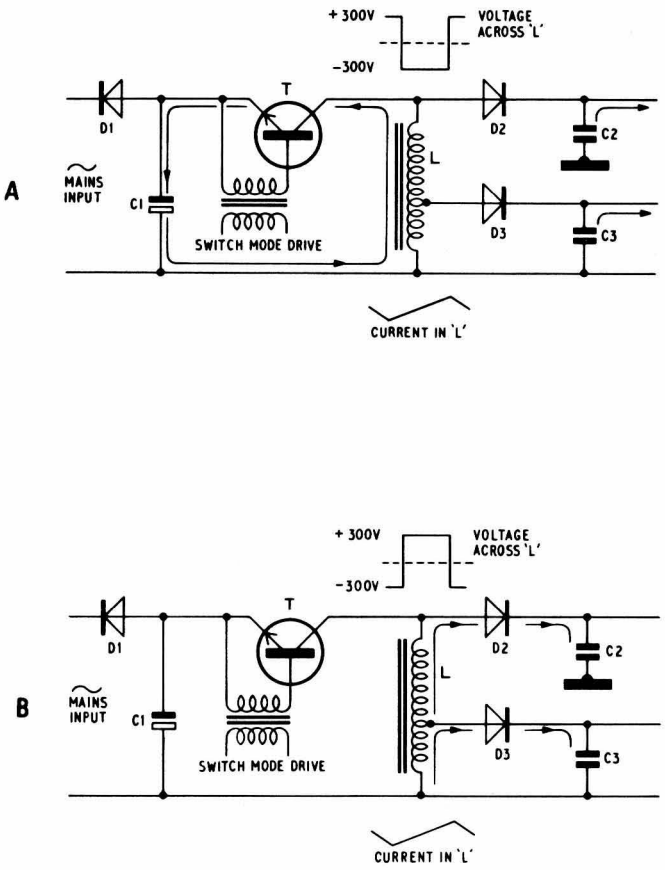


Fig. 3.2

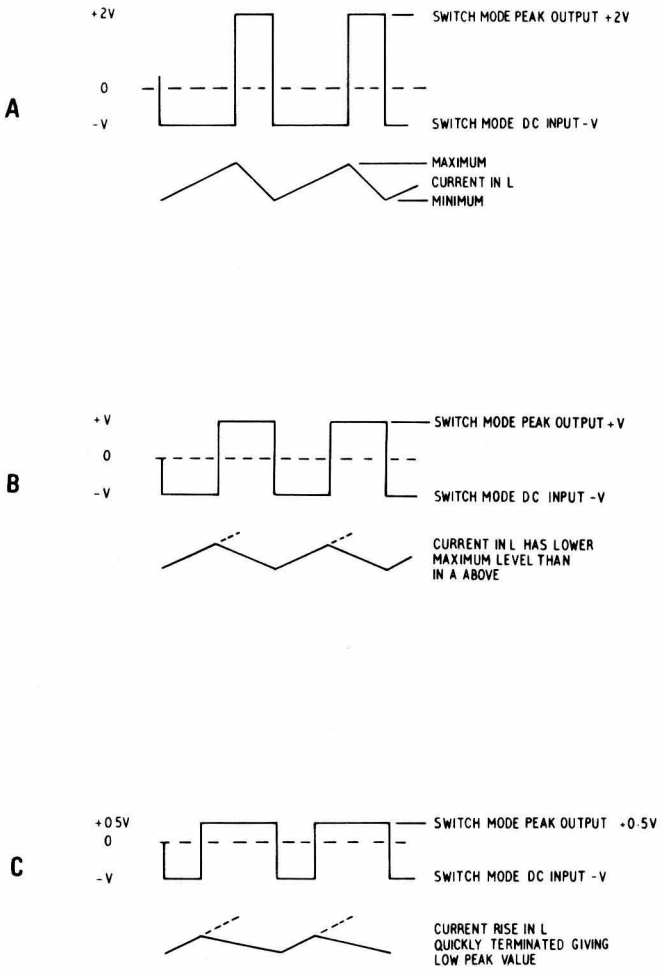


Fig. 3.3

In practice VT301 cannot turn off instantly but as soon as the collector current starts to fall the collector voltage will commence its rapid swing from a negative to a positive value. Precautions are therefore necessary to prevent VT301 dissipating too much power during this transitional period and W361, R362, C362 are included for this purpose.

When switching transistor turn off is initiated, the junction C362, T361 swings less negative and then positive which causes W361 to become conductive. C362 and T361 form a series tuned circuit with low impedance and the rate of rise of voltage across VT301 is reduced and turn-off wattage in transistor VT301 reduced. At this point C362 is charged to approximately 500V with polarity as shown in Fig. 3.4. As soon as the output supply recitifiers start to conduct the junction C362, T361 falls in potential and W361 turns off leaving the charge on C362 to leak away via R362 during the next on-period of VT301.

Resistor TF306 and capacitor C307 are included to damp the primary winding of the driver transformer and thus prevent the production of high amplitude voltage transients when VT302 turns off. In the absence of damping, these transients might exceed the permissible collector voltage rating of VT302.

d. Overload Protection Systems

Fig. 3.5 illustrates some of the various functions contained within IC301 which include the generation and control of switched mode drive plus several protection systems which will be dealt with in this section. The first of these systems gives fast action protection against current overload and is known as the dynamic current limiter. Capacitor C363 (2.2μF) passes a ripple current at the switching frequency of 15.625kHz which is proportional to the current being taken by the load. Each current pulse will produce a positive-going voltage spike across R363 and a proportion of each pulse is fed via R324, R325 and TF305 to the dynamic current limiter section of the IC.

A fault condition in the receiver circuits may cause a sudden increase in the current drawn from the switched mode, and the regulation circuits will widen the mark-to-space ratio in an attempt to meet the additional demand. If the current demanded is greater than would be required for normal receiver circuit operation, the voltage spike into the dynamic current limiter exceeds a critical value and the on-period is terminated within 1μs, thus protecting the transistor from damage due to excess emitter-collector currents. This premature termination of VT301 conduction limits the energy being fed to T361 and if the overload condition continues the rail output voltage will fall.

Other protection circuits operate by controlling the voltage across C308 which in turn controls the Schmitt trigger mark-to-space ratio. With no voltage across C308 the switched mode on-period will be in the region of 1μs only giving a very low rail output voltage. If the upper plate of C308 is made progressively more positive with respect to chassis, the switched mode mark-to-space ratio widens until at 5V it attains its normal working value. Further increase to 7V will fire the C308 electronic switch which provides a low impedance shunt path and rapidly causes the voltage to fall to zero again, thus virtually shutting off the supply. Once operated, the discharge circuit can only be reset by switching the receiver off for a minimum period of approximately 2 seconds.

The control characteristics of the voltage across C308 are utilised to provide four protection functions. Firstly, at switch-on C308 charges slowly from the 13V stabilised supply via TF305 and reaches 5V after approximately 5 seconds, thus giving a slow and controlled rise in output current whilst circuit capacitors become charged.

Secondly, there is provision in the dynamic limiter for a positive voltage output to be produced during periods of current overload. This positive voltage charges C308 via 'R_d' and if present for a period defined by the severity of the overload which exceeds a few seconds, will cause the electronic switch to fire thus turning off the output. This action provides a permanent overload trip facility.

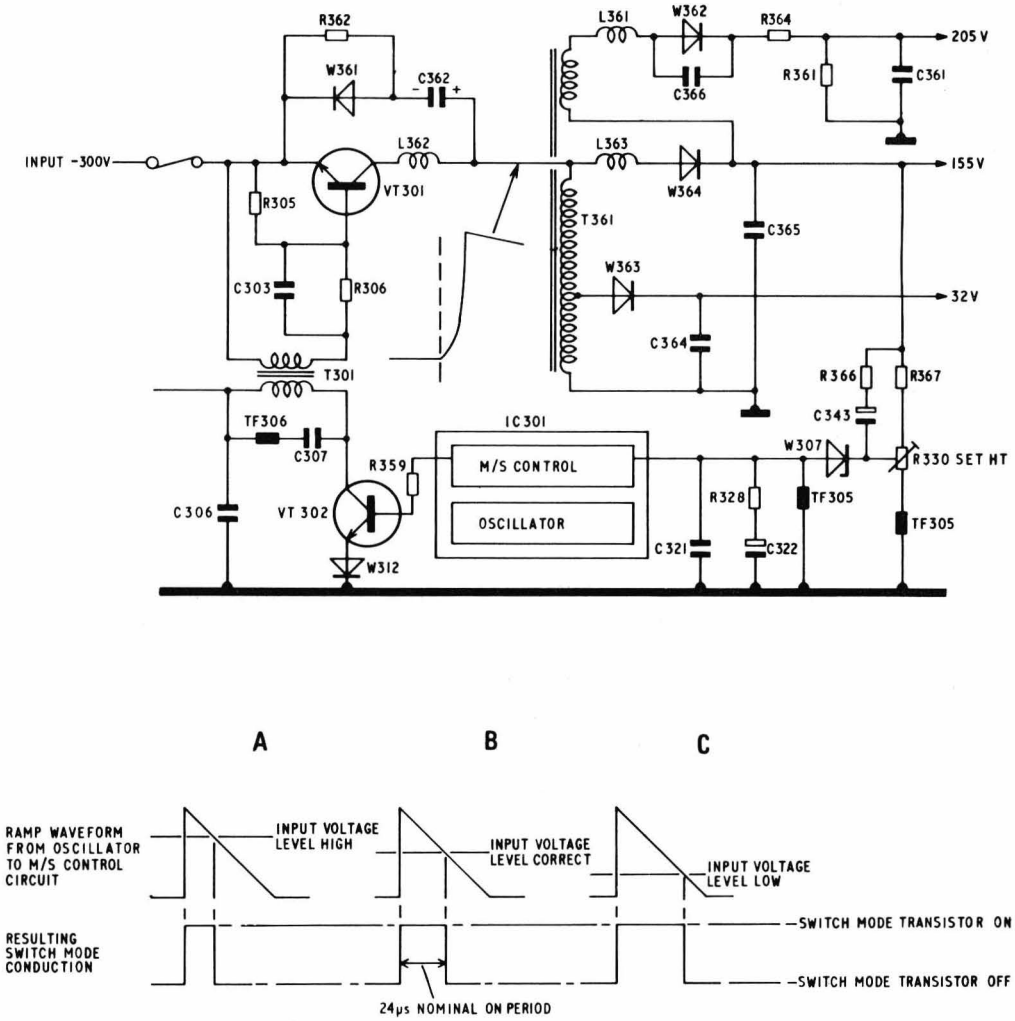


Fig. 3.4

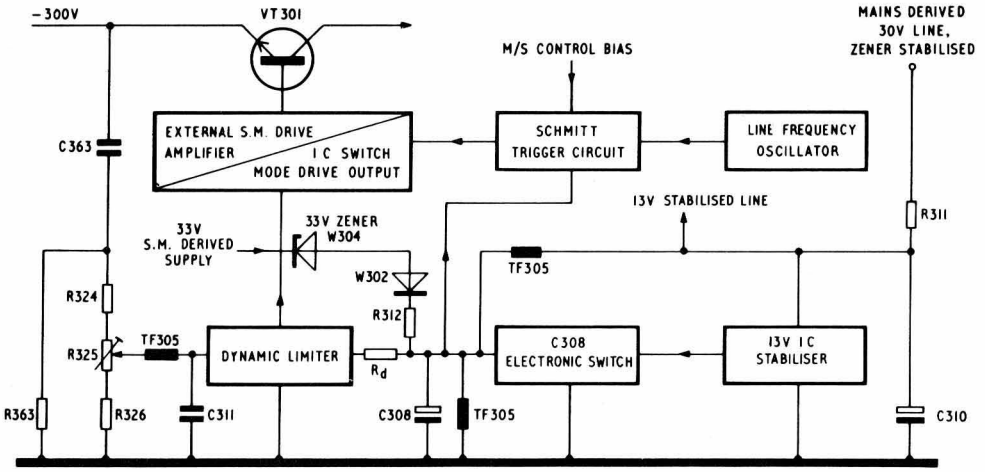


Fig. 3.5

Thirdly, a 33V zener diode W304, a diode W302 and resistor R312 are connected between the 32V switched mode derived line and C308. If the 32V rail exceeds 40V for any reason, conduction of W304 will raise the voltage across C308 above the critical level and firing of the electronic switch will again shut down the circuits.

The fourth action is to protect the switching transistor from failure due to operation in a non-saturated condition if the voltage supplies for the drive circuits fall below their correct values. Fig. 3.5 shows that the IC contains an internal 13V stabiliser system and if the supply input falls below 12.5V, so that the stabilisation action ceases, the C308 electronic switch will fire thus preventing any damage to VT301. In addition to providing general protection the circuit will ensure correct shut down of the switched mode section whenever the receiver is switched off.

e. Additional Switched Mode Derived Supplies

Fig. 3.6 shows the mains derived 50V and 30V rails, the 205V, 155V and 32V switched mode derived rails and some additional feeds with their own stabilisers which are obtained from the two latter switched mode output rails.

The 155V, switched mode output supplies only one subsidiary rail; 33kΩ resistor R157 ieeds a current of 3mA to 4mA through IC151 which is a monolithic integrated circuit stabiliser, type ZTK33CDPD. There will be approximately 33V across the device which will remain highly stable despite changes in input voltage, temperature and load current. This voltage is used to feed the variable capacity diodes in the tuner unit.

The 32V switched mode output is taken via a 10Ω resistor R159 to IC152 which is a monolithic integrated circuit stabiliser type μA7824. This device contains 17 transistors on a single chip and will supply 24V at output currents up to 1A with ripple rejection of approximately 60dB. In addition, it incorporates internal thermal overload protection and if the output is short-circuited will deliver only 150mA.

The 24V output from the IC is used to feed most of the small signal circuitry as shown, but in addition it supplies current to Zener diode W151 via R158 to provide a highly stable 12V rail for the tuner transistors and IC101.

The 32V switched mode output is separately decoupled by R341 and C408 to give a special 30V supply for the field oscillator, driver and output circuits.

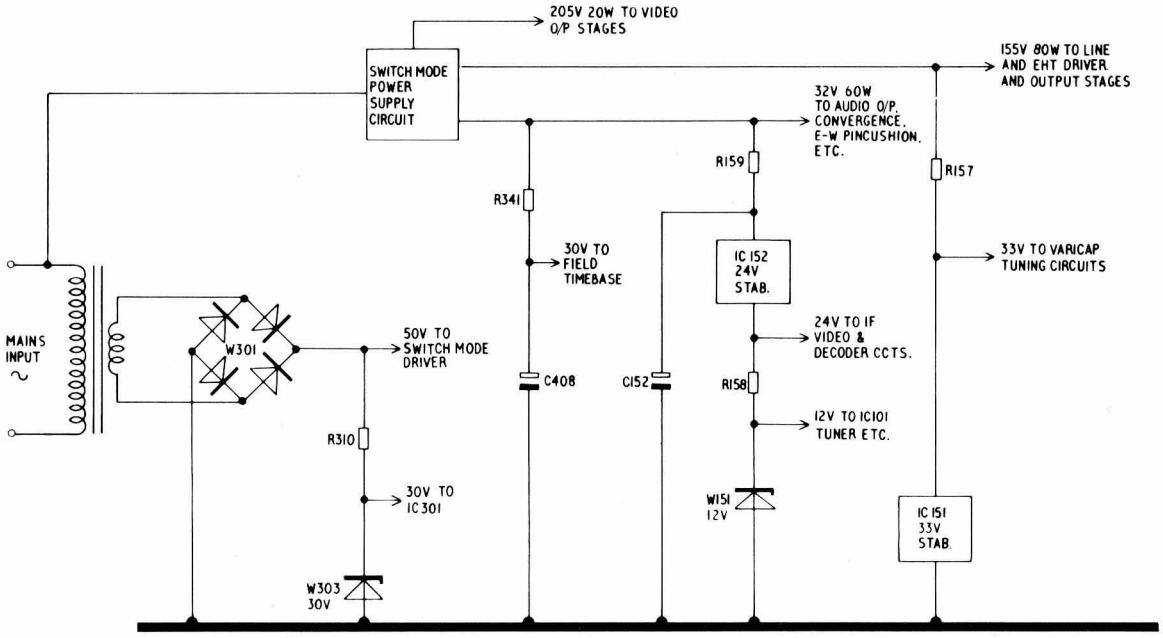


Fig. 3.6

Section 4. TUNER, CHANNEL SELECTOR AND BAND-CHANGE, IF AMPLIFIER, VISION DEMODULATOR, AGC AND AFC SYSTEMS

Refer to introductory notes on page 3

a. Tuner Unit

The combined VHF/UHF tuner plugs into a special socket on the signal board adjacent to the IF module, so that the length of interconnecting leads is kept to a minimum. It covers Band I (47MHz to 88MHz), Band III (174MHz to 230MHz) and the UHF bands (470MHz to 860MHz).

The components are mounted on a low-loss printed circuit board which is housed in a rectangular metal screening box. The two aerial input leads are connected to feedthrough insulators at the box ends and a row of feedthrough capacitors along the bottom edge carry AGC, tuning, band switching and supply voltages as shown in Fig. 4.1.

The tuner requires transistor supply voltages of +12V, a switching voltage of +12V, AGC voltages, variable from +2.4V (full gain point) to about +7.5V (maximum AGC) and a tuning voltage, variable from +0.3V to +28V.

b. Channel Selection and Band-Change Circuits

The AFC control voltage is taken from pin 11 of IC101 and fed to the base of VT107 (see Fig. 4.1). This transistor operates as an emitter follower giving a low impedance source for the control voltage to reduce the effects of voltage offset back to the AFC source over the range of the tuning potentiometer. The emitter of VT107 is approximately 5.6V positive with respect to chassis and thus cannot be directly connected to the tuning potentiometer isolation diodes W2A, etc, as these would be cut off at slider positions producing less than 6V above chassis. To overcome this problem, a 5.6V zener diode W105 is incorporated in the emitter circuit of VT107 and R129 is adjusted so that the AFC input to R20 is at zero voltage with respect to chassis when the receiver is correctly tuned.

The required AFC voltage swing into R20 will be between +6V and -6V so a negative bias supply is required. This is obtained as shown in Fig. 4.1 by application of a negative-going flyback pulse to a rectifying and doubling circuit W154, W155, W156, etc, which produces a-60V DC output. Resistor R153 feeds this negative potential to R20 and network R154, R155, R156 applies a small negative bias to W2A, B, C, etc, to ensure conduction when tuning voltages between 1V and 0.3V are present.

Correction for the variable AFC pull-in characteristic over the frequency range is made by the network Z1, Z2, W6, R18, R19. At tuning voltages between 1V and 6V when the AFC control at point A goes positive, the diode W6 will cut-off thus increasing the feed impedance by bringing the resistance of R19 into circuit. At higher tuning voltages, or with negative AFC action, W6 will remain conducting.

When the tuning voltage exceeds 19V the resistance of Z2 falls and this takes over from R18 as the determining feed impedance. Z1 is included to give a good compromise AFC hold-in to pull-in ratio

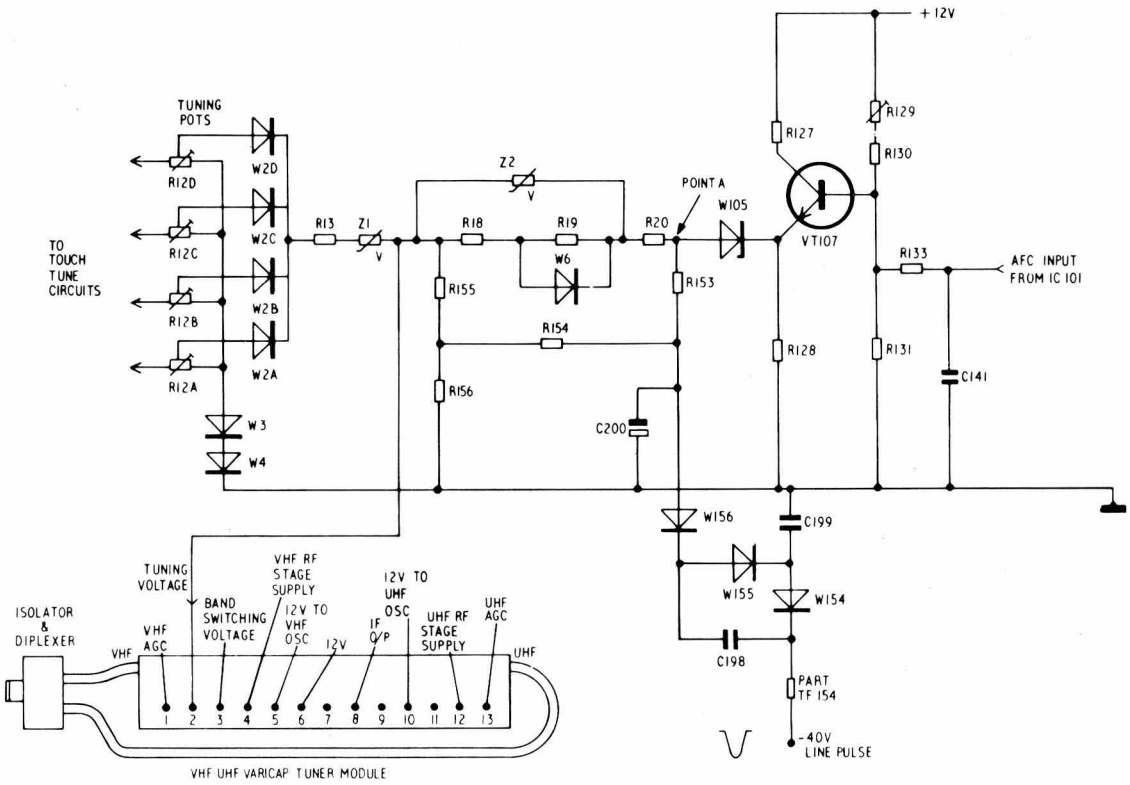


Fig. 4.1

at low tuning voltages without problems due to excessive range when tuning voltages between 6V and 17V are being used. AFC action is defeated for tuning purposes by simply shorting R20 to chassis through a suitable switch.

Band-change switching is accomplished by the circuit shown in Fig. 4.2. Each Programme-Selector Circuit has an associated three-position switch which may be operated with the tuning knob via a clutch mechanism. The switch positions are: upper contact Band I, centre contact Band III; and lower contact Bands IV and V, UHF.

When a channel is selected, the voltage from the top of the appropriate potentiometer is fed, via an isolating diode and three-position switch, to one of the switching transistor base circuits. If Band I operation is required, VT5 is saturated and supply current flows through the transistor to the VHF oscillator supply output. Similarly for UHF operation, VT7 is saturated and connects the 12V input rail to the UHF oscillator supply output. Transistors VT6 and VT8 provide switching of the tuner coils between Band I and Band III. When operating on Band I the tuner unit has an internally produced negative voltage on its Band I/III switching input, and it was therefore necessary to use a pnp switching transistor VT8 to avoid the collector-base junction becoming forward biased.

Diodes W8, W9 and W10 perform the following logic functions. For Band I operation VT5 is on but W8 is reversed biased so VT6/VT8 remain off. For Band III operation, W8 and W9 are forward biased, causing VT5 and VT6/VT8 to be turned on. For UHF operation, W10 is forward biased bringing VT6/VT8 on as it is necessary to have the Band III coils in circuit to prevent random pick-up problems and VT7 is also on to complete the UHF oscillator supply.

AGC switching between the two tuner sections is achieved by turning on diodes W11 or W12 by feeding positive voltage from the respective oscillator supplies, thus completing the appropriate AGC circuit.

The touch-tuning circuit consists of a 24-pin MOS integrated circuit, which incorporates sensing amplifiers and latching circuits, as shown in Fig. 4.3. One side of each touch-pad is fed from the 150V line via two 4.7MΩ resistors R1 and R2. The resistance of a finger bridging the plates of a touch-pad can be several tens of megohms and it is for this reason that a high input impedance MOS device is required for sensing. Two further 4.7MΩ resistors, R3 and R4, and a 10MΩ resistor R5 form a divider across the input, and C1 is included to prevent induced pulses due to CRT flashover causing random channel changes.

When the signal at any input exceeds 15V the internal latching circuit operates causing the input pin to be pulled up to 34V and also connects the 35V stabilised varicap feed to the appropriate tuning potentiometer. The IC will remain latched in this manner until a releasing signal of more than 15V appears on another input pin. When the receiver is switched on, the IC will always select input No. 1 which can be used for the customer's favourite channel.

VT2 in Fig. 4.3 is a shunt stabiliser to provide 36V which uses the 35V varicap rail as a reference potential. When changing channels it is desirable to switch AFC off and mute the sound channel and these operations are performed by VT4 and VT3 respectively. A positive-going mute signal is obtained from the IC whilst channel selection is in progress and this causes the Field Effect transistor VT4 to conduct heavily, connecting point 'A'. Fig. 4.1, in the AFC line to chassis. An FET is required for this function as the AFC Control voltage can swing both positive and negative with respect to chassis. When transistor VT3 conducts, it provides a low impedance shunt across the DC volume control circuit of IC154 and thus reduces the volume to minimum.

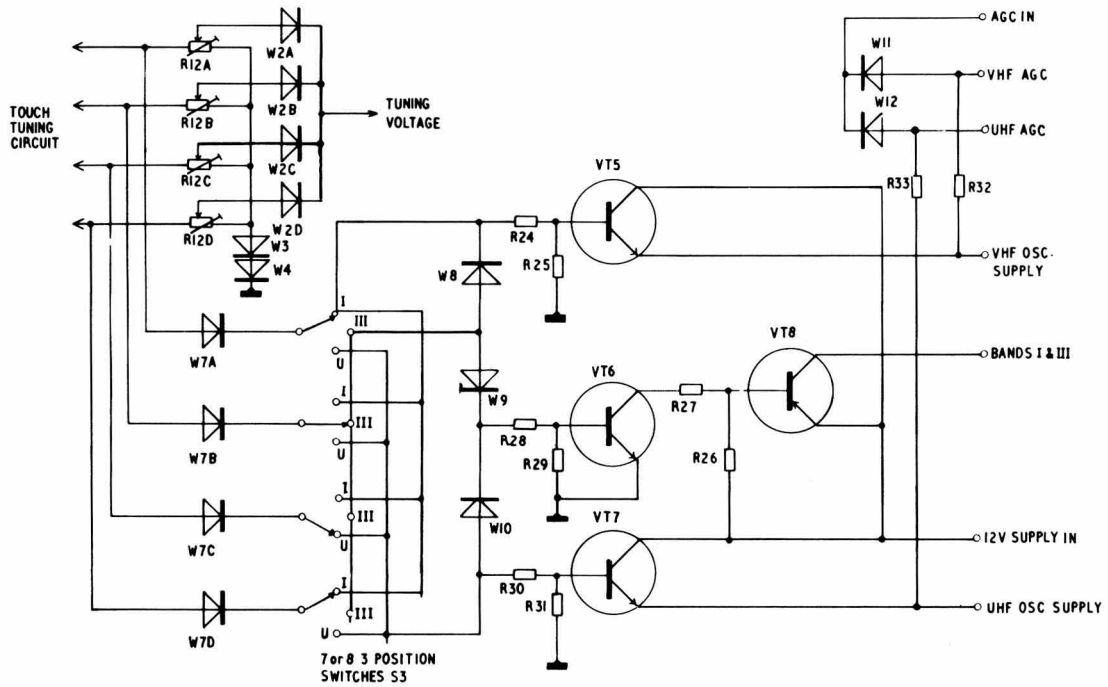


Fig. 4.2

c. IF Amplifier and AGC System

The IF amplifier and associated automatic gain control circuits are shown diagramatically in Fig. 4.4. Signals from the tuner are taken through a bandpass network which is followed by adjacent channel sound and vision traps and the first required sound channel trap to the 3-Stage IF amplifier. The first and second IF transistors VT101 and VT102 have forward AGC control voltage applied to their bases via 470Ω resistor R103 and 1.8kΩ resistor R109 respectively. The preset control R104 adjusts the gain of the two transistors, and specifically when the delayed gain control of the tuner is about to commence. The third IF amplifier transistor VT103 operates at a fixed gain. All three IF stages have tuned collector loads which are heavily damped by parallel resistors,and aided by feedback in R108,give a broad flat frequency response which is not seriously affected by AGC action.

The third IF stage is followed by a triple section band-pass coupling network which also includes a 41.5MHz trap intended to reject any strong local signals near this frequency, such as the sound carrier of UK Channel 1 transmissions.

Following the bandpass network, signals go via the main required sound channel trap, which consists of L112, C131, C132 and R123, through C130, R122 to the signal input pin of demodulator IC101.

Positive-going, sync-tip-derived AGC, line gated, with amplitude which varies in proportion to the received signal strength, is produced at IC101 pin 5. After smoothing, it can be used to provide forward AGC bias for the IF stages. If simple RC smoothing was used, a long time-constant would be required to remove the field-frequency component present in the pulses and this would result in slow acting AGC. Signal variations due to reflections from aircraft and traffic can be of a very rapid nature and fast acting AGC is necessary to maintain a steady picture under these conditions. Transistor VT106 and its associated components provide a fast acting AGC system which can deal effectively with large signal fluctuations at a rate of 15Hz–20Hz, but which retains a long time-constant under normal conditions to provide adequate filtering at field frequency. W106 removes some of the field-frequency component present in the AGC at the internal amplifier and C134 removes the line rate components.

Referring to Fig. 4.4 it will be noted that 100μF capacitor C133 charges from the 12V supply via 1kΩ resistor R124. This causes the AGC line to become positive with respect to chassis and when it reaches approximately 5V zener diode W103 will conduct. W104 is also forward biased and the current through R124 which was charging C133 is now diverted via the IC to chassis.

As the input from pin 5 becomes more positive, indicating an increase in received signal strength, the AGC line will also become more positive, increasing the current in controlled transistors VT101 and VT102, and reducing the IF gain by forward AGC action. Zener diode W101 is necessary to provide a 5.6V DC step-down thus reducing the base voltages of VT101 and VT102 to a level which permits the emitters to be directly connected to chassis.

If the received signal suddenly increases in strength, the positive input will follow, reach a large amplitude and turn on VT106 which then passes collector current to rapidly charge C133. A sudden fall in signal level will result in C133 being rapidly discharged through W103 and W104 to the 5V level as previously described. The requirement for an AGC system which is quick acting when large signal fluctuations occur but which retains a basic long time-constant are thus satisfied.

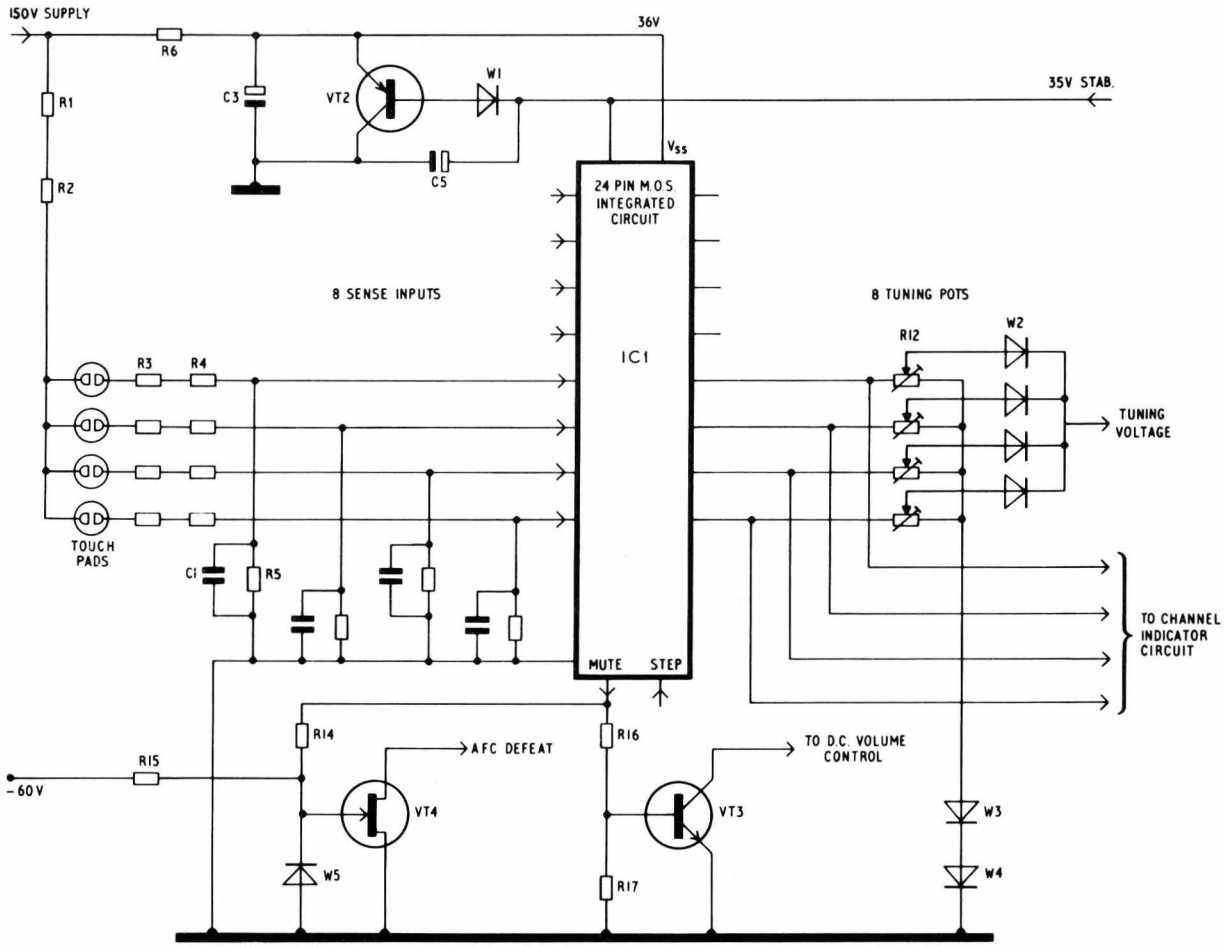
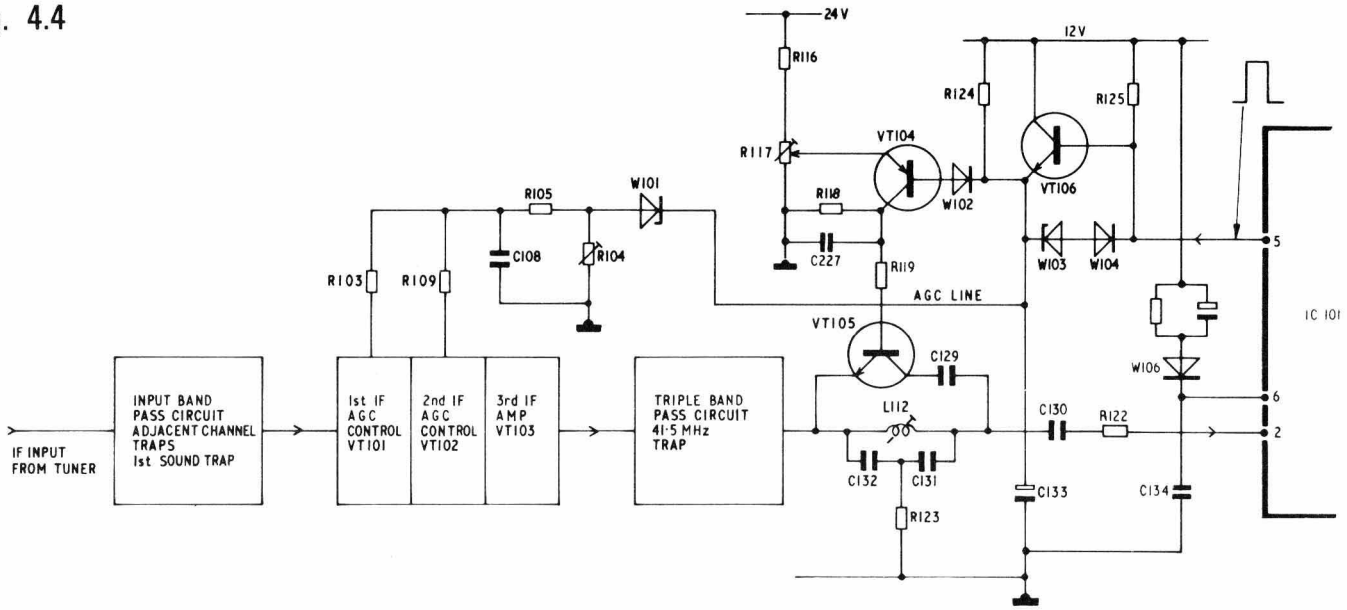


Fig. 4.3

Fig. 4.4



When the receiver is operating on signals from distant transmitters, there may be periods when deep fading causes the picture to cease to be of entertainment value. It is an advantage if sound reception can be maintained under these conditions and the method of achieving this is to temporarily reduce the degree of sound carrier rejection in the IF amplifier. It will be noted from Fig. 4.4 that the base of VT104 is connected to the AGC line via W102. Preset potentiometer R117 is adjusted so that VT104 remains cut-off under normal conditions, but if very weak signals are indicated by the AGC line falling towards 6V the base becomes negative with respect to the emitter and collector current flows, causing the base of VT105 to become more positive. VT105 turns hard on and connects the 30pF capacitor C129 across the sound trap, which effectively detunes the circuit and greatly reduces attenuation of the sound carrier signal.

d. Synchronous Demodulator IC101 and Associated Circuits

After passing through selectivity networks following VT103, the IF signals arrive at pin 2 of IC101 with an amplitude of approximately 70mV rms. IC101 is a monolithic silicon device, type TCA270B, and contains an IF synchronous demodulator, video amplifier, noise inverter and buffer stages giving video outputs of both polarities. In addition, there are sections to provide an amplified AFC control voltage and AGC outputs suitable for IF and RF stages which incorporate npn transistors.

Functions within the IC are illustrated schematically in Fig. 4.5. which also includes peripheral components and pulse generating transistor VT151.

The simple diode half-wave envelope demodulator has a number of shortcomings when used as video detector in television receivers. For example, the curvature at the bottom bend in the diode characteristic causes white signal crushing and distortion of saturated colours unless very high IF levels are used, whilst the inherent non-linearity results in sound and chroma signals mixing to produce familiar beat patterning in coloured picture areas. The applied synchronous demodulation is extremely linear and so these problems do not arise.

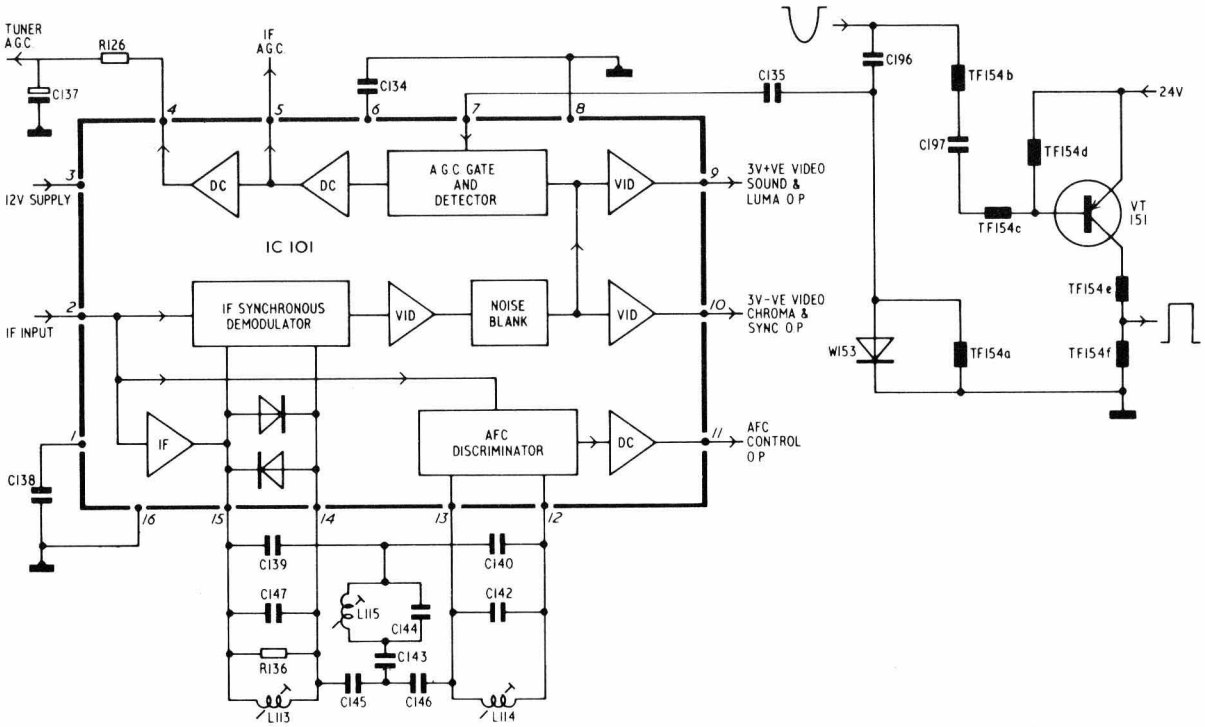


Fig. 4.5

After entering the IC via pin 2, the IF signal is amplified and then brought out on pins 14 and 15 to be applied across tuned circuit L113 and C147. Internal diodes are connected across the pins, as shown, and these limit the waveform giving a constant amplitude switching signal which may be varied in phase by adjustment of L113. The IF input signal is applied to a demodulator section of the IC and gated by the switching signal, so that alternate half-cycles of the IF are passed. The process is effectively one of full-wave rectification and both half-cycles contribute to the output, giving high efficiency and ripple frequency at twice the IF.

The demodulator is followed by a video amplifier and noise pulse blanking circuit to minimise white spot interference. Separate buffer stages provide a 3V pp positive-going video signal with sync tips at 3V DC from pin 9, and a 3V pp negative-going video signal with sync tips at 9V DC from pin 10.

Voltage from across the demodulator tuned circuit C147 and L113 is fed through 1pF capacitors C139, C140, C145, C146 to the AFC discriminator tuned circuit C142, L114. A sound IF trap circuit consisting of C143, C144, L115 is connected across the coupling capacitors to bypass any discriminator input at this frequency, thus preventing erroneous AFC lock onto the sound carrier. The low value coupling capacitors together with the discriminator tuned circuit form a frequency-conscious phase-shift network so that inputs on pins 12 and 13 will change in phase relative to the signal from pin 2 as its frequency changes. Phase comparison in the discriminator produces a DC voltage which is proportional to this phase difference, and after amplification this is passed to AFC output pin 11 from where it is applied to the base of VT107 as described in previous Section 3b.

In addition to the functions already described, IC101 also contains an AGC detector circuit, followed by amplifiers giving outputs suitable for feeding the IF and tuner RF stages with control bias via filter networks. Normal AGC operation is controlled by a gating pulse and this is derived from the shaping network shown in Fig. 4.5 as follows:

A 40V negative-going line flyback pulse is fed to a differentiating circuit consisting of C196 and TF154a. The resulting waveform is 5V negative for a period equal to and coincident with, the line sync period, and it is this negative pulse which performs the AGC gating function. The positive output pulse from the differentiator is not required and is clipped by diode W153. Positive-going rectangular gating pulses are required in the luminance and chrominance channels and are generated by VT151. The negative-going line flyback pulse across the differentiating network is fed to the base of VT151 via TF154 b & c and drives the transistor into saturation. When this occurs, collector current flows through TF154e and TF154f, and a well defined rectangular pulse is produced as shown.

The AGC detector selects the line sync pulse in a gating circuit and uses its peak amplitude as a measure of received signal strength. Separate amplifiers within the IC provide AGC feeds for the IF and tuner circuits. The IF feed is taken to a special fast AGC circuit which is described in Section 4c, and the tuner feed goes via filter network R126, C137.

If the receiver line oscillator should stop running or be off-frequency, the sync gating operation will fail, but in this case the AGC detector will continue to function using the peak sync level thus preventing an overload or blocking condition of the amplifier stages.

Section 5. CHROMINANCE DECODER AND VIDEO-FREQUENCY CIRCUITS

a. Basic Decoding and Video Drive System

The chrominance and video-frequency signal processing in the 4000 series design is carried out by three silicon monolithic integrated circuits as shown in Fig. 5.1. Chrominance (chroma) signals from IF demodulator IC101 are fed via suitable tuned input circuits to chrominance processing IC156 which is a specially designed type TBA395. This device produces a 7.8kHz identification waveform, 4.43MHz reference output and fully blanked chrominance signals.

Luminance (luma) signals from the IF demodulator pass via a 0.6μs delay line to IC155. The chrominance signal output from IC156 is also fed to IC155 and variable DC bias inputs applied to the IC to control brightness, contrast, saturation and beam limiting. IC155 has been specially developed to perform this luminance and chrominance control function in the 4000 design and has type number SC9505P.

Signal and reference outputs from both preceeding devices are applied to a third IC (IC157) type SN76227N. This unit contains synchronous demodulators which produce colour-difference outputs, a matrix circuit for the recovery of G–Y, a luminance adding circuit which provides R, G and B signals and emitter followers to provide low impedance drive for the following video output stages. The video output amplifiers use 250V transistors, type BF258, and can produce 120V pp drive at each CRT cathode.

All three integrated circuits derive their supplies from the 24V rail via suitable dropping resistors. IC156 has an internally stabilized main rail which holds the input voltages at 8.2V. IC157 operates at the 24V level but also incorporates a stabilizer to provide internal supplies at lower voltage levels. The three video output stages have a special switched mode 205V supply.

b. Chrominance Processing IC156

(see also f. Alternative Chrominance)

Negative-going video plus chrominance signals are taken from pin 10 of the IF demodulator IC101, through a 4.43MHz bandpass circuit and 5.5MHz sound trap, to input pin 3 of IC156 as shown in Fig. 5.2. After entering the IC, the chrominance signal is passed through an amplifier circuit which is gain controlled by ACC bias. Set ACC control R226 adjusts DC conditions within the loop so that a correct output level is achieved and ACC action will ensure that the burst portion of the waveform will remain at a substantially constant amplitude.

After amplification, the chrominance signal is taken to amplifiers which are controlled by the line-derived switching pulse produced by VT151 as described in Section 4c. From these circuits are obtained a burst-blank chroma signal, which is passed to the colour processing section and a gated-out burst, which is passed to the colour killer and reference generator sections.

The 4.43MHz chrominance reference signal is generated by an oscillator section within the IC which utilises crystal XTL151, plus trimming capacitor C207 to determine the free running frequency. Oscillator waveform,and frequency and phase of the burst,are compared in a phase detector circuit and any difference-signal will produce an error voltage output which is used to correct the oscillator. Precise balance in the phase detector loop is achieved by adjustment of preset control R224. C209, C210 and R222 determine the loop time-constant. Line derived pulses are used to trigger a bistable circuit which runs at half-line frequency and provides drive for the PAL switching in IC157. As the bistable may be in one of two states during a particular line it is necessary to compare its waveform with the line identification signal from the phase detector. If the comparator detects an incorrect switch condition it inhibits the bistable for one operation, thus restoring correct PAL synchronisation. Another important function of the comparator circuit is to control the colour killing operation. An inhibit signal is supplied to the killer circuit which prevents any output from pin 1 when monochrome or too weak colour signals are being received. Only when the reference generator is frequency- and phase-locked to the burst, and when the PAL switching is in the correct phase, will the inhibit be removed.

Pins 4 and 12 of the IC provide connection points for external .047μF decoupling capacitors. The amplitude of burst signals at the phase detector is an indication of chrominance signal-strength and is used in the comparator to produce ACC control bias.

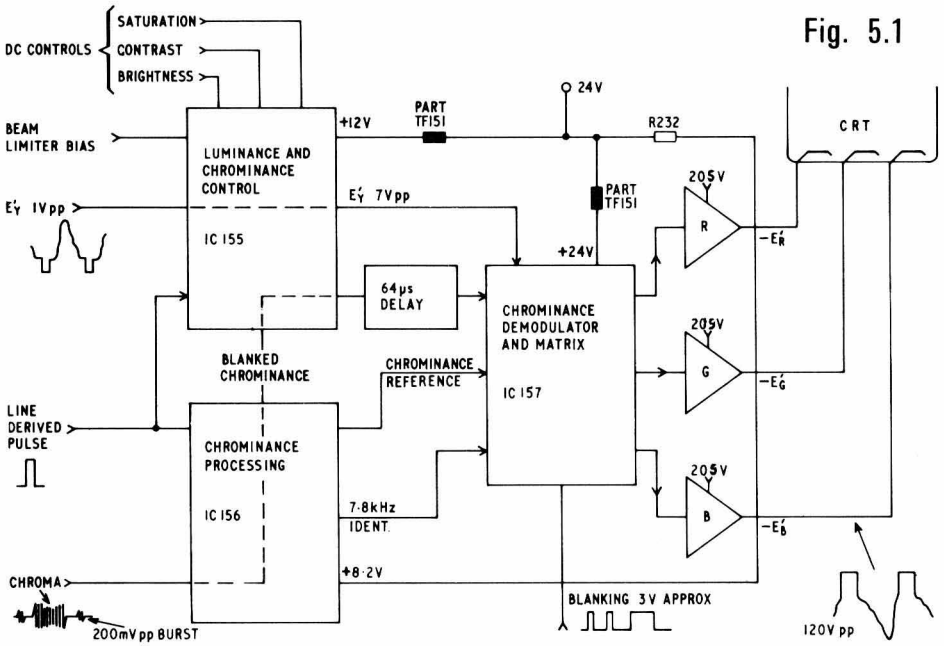
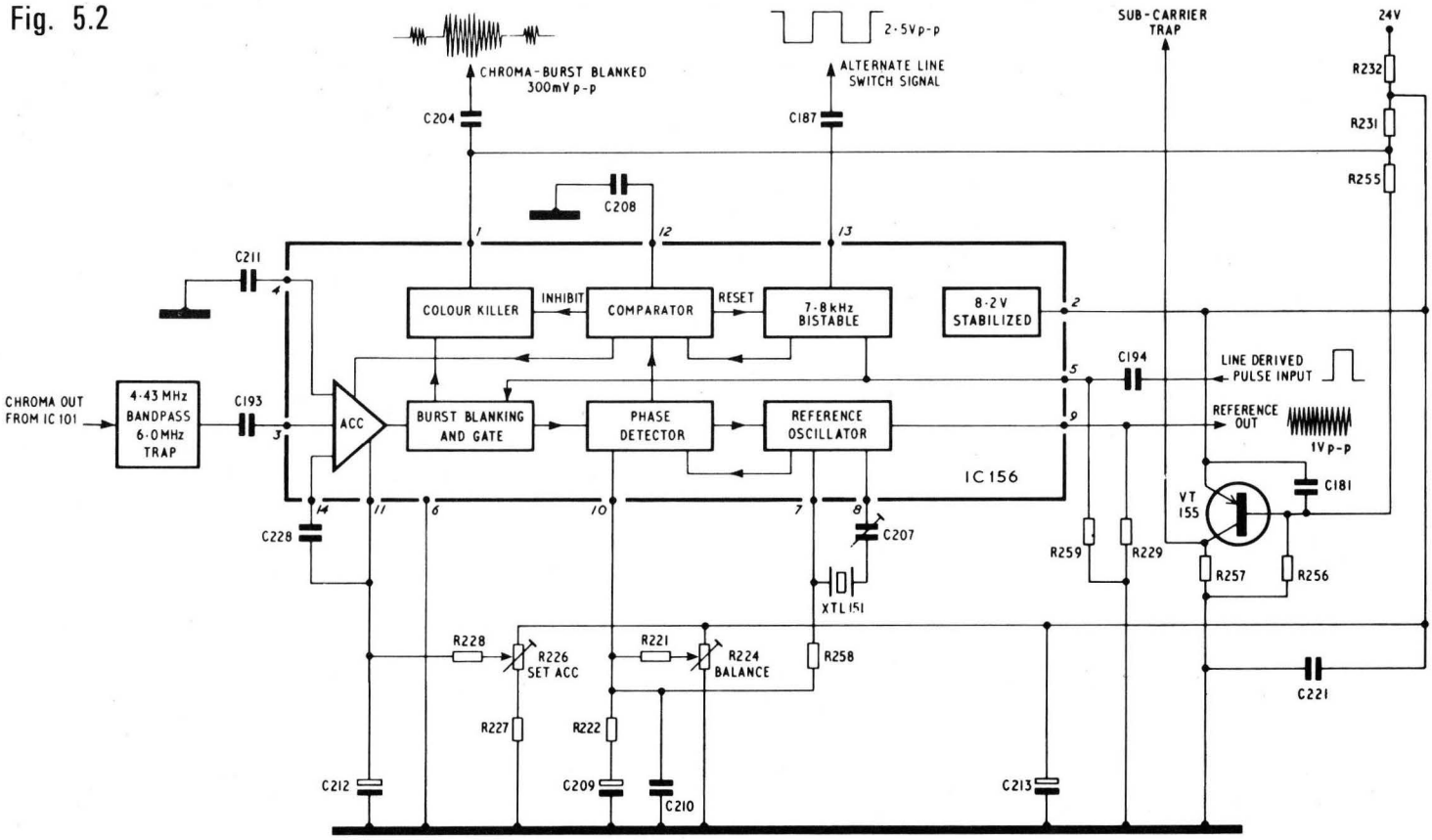
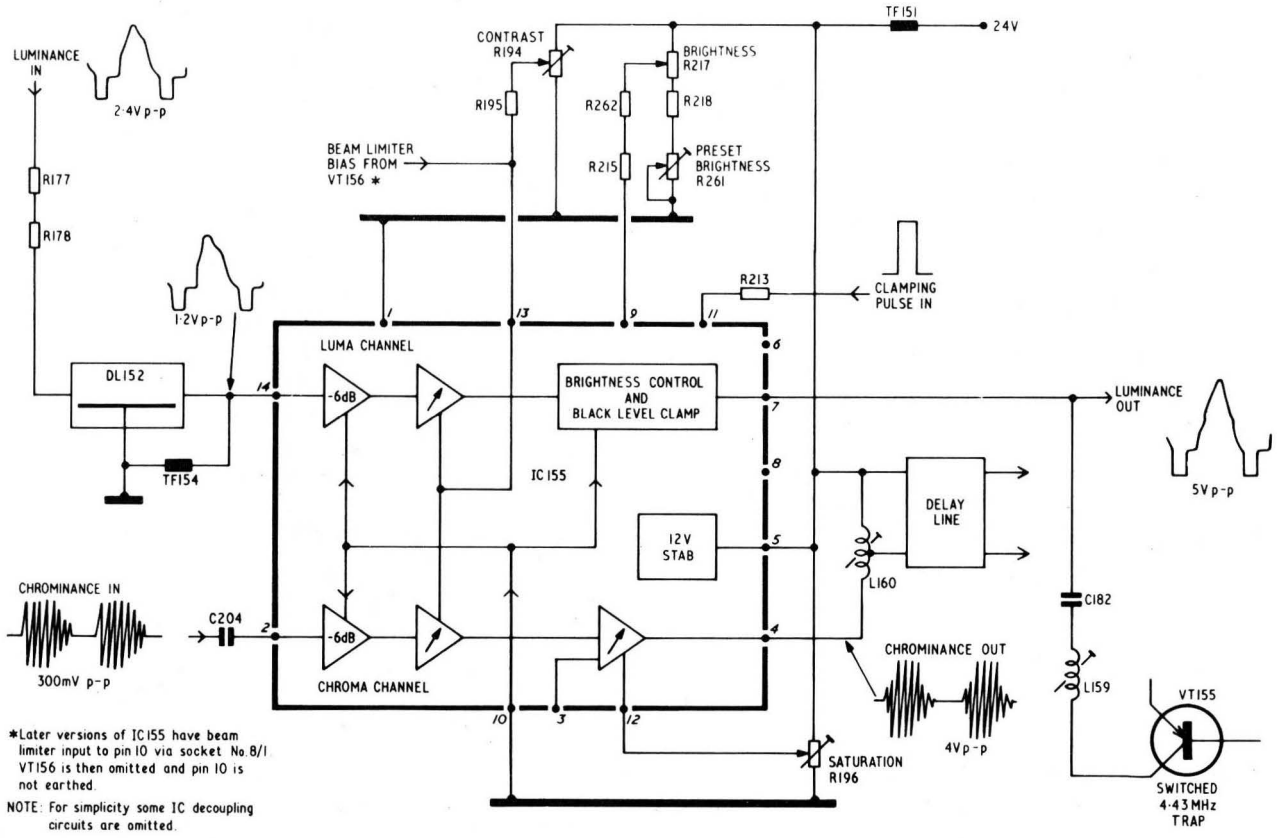


Fig. 5.1

Fig. 5.2





*Later versions of IC155 have beam limiter input to pin 10 via socket No.8/1. VT156 is then omitted and pin 10 is not earthed.

NOTE: For simplicity some IC decoupling circuits are omitted.

Fig. 5.3

c. Luminance and Chrominance Control IC155

Positive-going luminance signals of approximately 2.4V pp are obtained from pin 9 of IF demodulator IC101 and pass via a DC blocking capacitor, R177 and R178 to the luminance delay line DL152 as shown in Fig. 5.3. TF154 provides correct termination for the delay line impedance between IC input pin 14 and chassis. As a result of passing through the delay line, the luminance signals at the IC input are delayed by approximately 0.6μs relative to the corresponding chrominance signals.

The block diagram of IC155 in Fig. 5.3. shows the three basic luminance control functions in the upper section and three related chrominance control functions in the lower section. The luminance channel is fed via pin 14, as described, and a burst-blanked chrominance signal of approximately 300mV pp from the preceeding IC156 is applied to pin 2 via C204.

After entering the IC both luminance and chrominance signals pass through variable attenuator stages which permit the signal output level to be progressively reduced by application of beam limiter bias or contrast control at pin 13. As the luminance and chrominance amplifier gains are simultaneously controlled by the voltage from R194, any adjustment to contrast level will be accompanied by a similar variation in chrominance level, and visible picture saturation will remain the same.

In the luminance channel, the contrast control amplifier is followed by a black level clamp and brightness control circuit. A line-derived pulse from VT151 is fed to pin 11 via R213 and a variable DC bias from the brightness control divider is fed to pin 9 via R262. R261 is the preset brightness. When the line pulse occurs, a clamp circuit operates and DC restores the luminance signal to the voltage from the brightness control slider. Changes in the setting of R217 cause the luminance signal black-level to rise or fall, thus giving an effective change in the brightness of the displayed picture.

Luminance signals leave the IC via pin 7 with an amplitude of approximately 5V pp for normal levels of CRT drive. A 4.43MHz trap L159–C182 is connected across the luminance signal path to attenuate dot patterning effects due to the modulation on the chrominance sub-carrier. When the receiver is operating on monochrome signals, the trap is not required and if left in circuit would cause a slight loss of definition on some scenes. Transistor VT155, in series with the trap, has its base fed with a DC bias from IC156 pin 2 which cuts the transistor off during monochrome reception but causes it to saturate and switch in the trap during colour reception.

In the chrominance channel, after the contrast control amplifier there is a further stage which has its gain determined by a variable DC bias from the slider of saturation control R196. Chrominance signals leave the IC via pin 4 with a typical amplitude of 4V pp. The chrominance delay line is a multipath glass type and a matrix circuit provides U and V signals for the decoder IC which follows.

The beam limiter circuit restricts the maximum contrast available so that beam current does not exceed its preset maximum. The threshold, i.e. the mean beam current at which limiter operation commences,is set by R348 (beam limiter preset) on the power board.

If for any reason the line-derived clamping-pulse failed, the displayed brightness would increase due to non-operation of black-level clamping within the IC.

d. Chrominance Demodulator and Matrix IC157

A block diagram of the chrominance demodulator and matrix IC157 is shown in Fig. 5.4 which also includes peripheral circuits and the blue video output stage (the red and green video output stages are similar). Separated U and V chrominance signals from the glass delay line circuit are fed via pins 8 and 9 to amplifier stages, which have gain ratios to compensate for the weighting factors used in the PAL system. Each amplifier provides two outputs which are in antiphase and drive the double balanced synchronous demodulators as shown. By using demodulators which operate on both half-cycles of the chrominance signal waveforms, it is possible to obtain positive- and negative-polarity colour difference outputs simultaneously and to double the ripple frequency so that filtering is simplified.

Reference signal for the demodulators is generated in IC156 and has a phase which is suitable for direct application to the U demodulators via pin 13. The V demodulators require a reference signal which is 90° phase-shifted relative to the U reference; and centre-tapped coil L163, together with C190 and R230, form a network which supplies a suitable voltage to pin 12. Correction for the alternate line phase reversal of the V chrominance component is achieved by effectively reversing the V reference on alternate lines and the 7.8kHz square wave, supplied from IC156 to pin 11 drives a half-line frequency switch which performs this function. The demodulators provide positive-polarity colour difference signals to feed the output circuits and negative-polarity colour difference signals for matrixing to produce positive G–Y signals.

Luminance signals are fed from IC155 to pin 3. C185 and L161 are series resonant at 5.5MHz to remove any residual sound carrier from the video channel. Positive-going blanking signals derived from the line and field timebases are supplied to pin 6. After inversion, to make them negative- going, they are effectively added to the luminance signal and ensure that this remains well below black level during scanning flyback. As the EHT generator is separate from the line output stage, a fault condition may result in the display of a bright vertical line instead of a complete raster on the CRT and a protection circuit is necessary to prevent this. The anode of diode W152 (see Fig. 5.4) is returned to a potential divider R198, W161 which is connected between the +24V rail and the -60V supply derived by voltage doubler from line flyback pulses. Normally W152 is non conductive, but if the -60V supply fails, indicating a line output failure, W152 becomes forward biased and the +24V supply causes the blanking input at pin 6 of IC157 to rise and extinguish the beam.

The blanked luminance signals are now added to colour-difference outputs, from the two demodulators and G–Y matrix to obtain RGB signals. Before these output signals leave the IC via pins 1, 2 and 4, they pass through emitter follower stages to provide a low-impedance, high-current source for the following video output transistors, VT152, VT153 and VT154.

e. Video Output Stages

Fig. 5.4. shows the blue video output stage directly coupled to pin 4 of IC157 via filter coil L166. The red and green video output stages are of similar design and have consequently been omitted from the simplified drawing. Transistors with a 250V collector-emitter rating are used and each stage has a video input of approximately 5V black-to-white, a gain of approximately 25, and can deliver 120V black-to-white CRT cathode drive.

Picture black level produces a signal which is about +9V above chassis on each of the output transistor bases and this gives a corresponding CRT cathode signal of 160V above chassis.

Each emitter circuit is fed from a 5.6V stabilised DC supply provided by W157 and R192 from the 24V rail. By carefully choosing this voltage and the values of emitter resistors TF153, R250 and R251 it is possible to achieve a satisfactory control of the video drive amplitude without causing significant changes to the DC conditions. Small adjustments of picture highlight drive can thus be made without requiring complete grey-scale tracking procedures to be followed.

Frequency compensation in each video output stage is provided by an emitter bypass capacitor (C216 in Fig. 5.4) which more effectively bypasses the emitter resistors as video frequencies increase, thereby reducing degenerative feedback and giving a rising gain characteristic. The small inductor of 150μH in series with each collector load (L169 in Fig. 5.4) increases the total load value at high frequencies giving compensation for the corresponding decrease due to stray capacities which shunt the load. Further compensation exists on the tube base assembly, e.g. L703 which splits up the capacity loading.

Gamma correction, i.e. an increase of gain with high-level video drive, is provided in the video emitter circuits : the blue channel thus has W160 and R270 across the emitter resistance so that above 3.3V, W160 conducts and the gain is increased due to R270 in parallel with TF153. There are similar circuits in the red and blue channels but emphasis is given to the green (R269 being lower in value than R268 and R270) to produce a more acceptable white. This circuit applies compensation when peak beam current drive is applied to the tube.

f. Alternative Chrominance Processing Panel (Fig. 5.5)

An alternative chroma panel is fitted in some receivers in place of IC156 and associated circuitry and operates as follows:

Composite chroma signals (nominal 200mV pp burst) from the take-off circuit, L152, L153 and L154, enter IC901 at pin 4 and are amplified via an ACC-controlled circuit to provide blanked chroma output at pin 9 and a gated low-impedance burst output of 1V pp at pin 12. The necessary 2.5V negative gating and blanking pulses at pins 13 and 14 respectively are generated from the line flyback pulse in the inverter-clipper stage VT904. R913 presets saturation.

Smoothed ACC is applied at pin 2 with the ACC loop gain internally adjusted from R902 with C902 decoupling.

The reference ident and ACC generation is carried out by IC902 with burst gating via R924.

The 1.5V pp burst at pin 5, obtained from IC901 via L901 and C908, causes the internal reference oscillator to lock: initial frequency adjustment is by the trimmer C917 and the balance of the internal phase detector is set by R934. ACC of approximately 2.2V for IC901 is available at pin 9, and ACC gain is set by R930.

IC903 contains the PAL flip-flop which drives IC902 pin 8 and is also taken out via C927 to drive the PAL switch in IC157. Line pulse at pin 4 triggers the flip-flop and it is stopped from running by conduction of W902. This occurs when the ident is in the wrong phase, resulting in a forward voltage on W902 via the zener W907 from pin 9. When correctly identified the voltage drops sufficiently to switch W902 off and hence keep the flip-flop running. The killer voltage at pin 7 of IC902, internally derived from the conditions at pin 11, rises from near zero to 6V during colour which is properly identified and 'unkills' chroma via pin 5 of IC901.

Reference output from pins 4 and 6 of IC902 is phase shifted in L902, C912 and

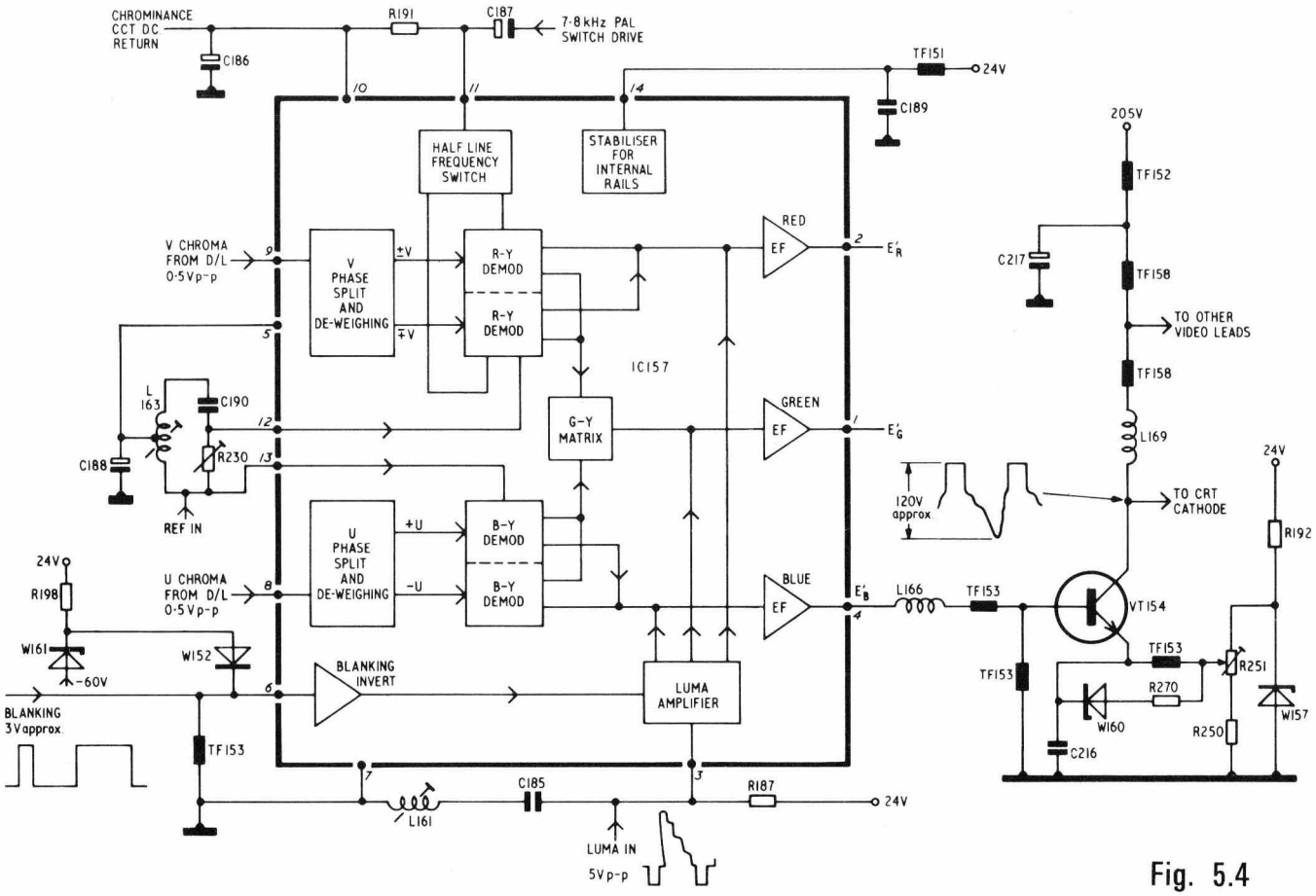
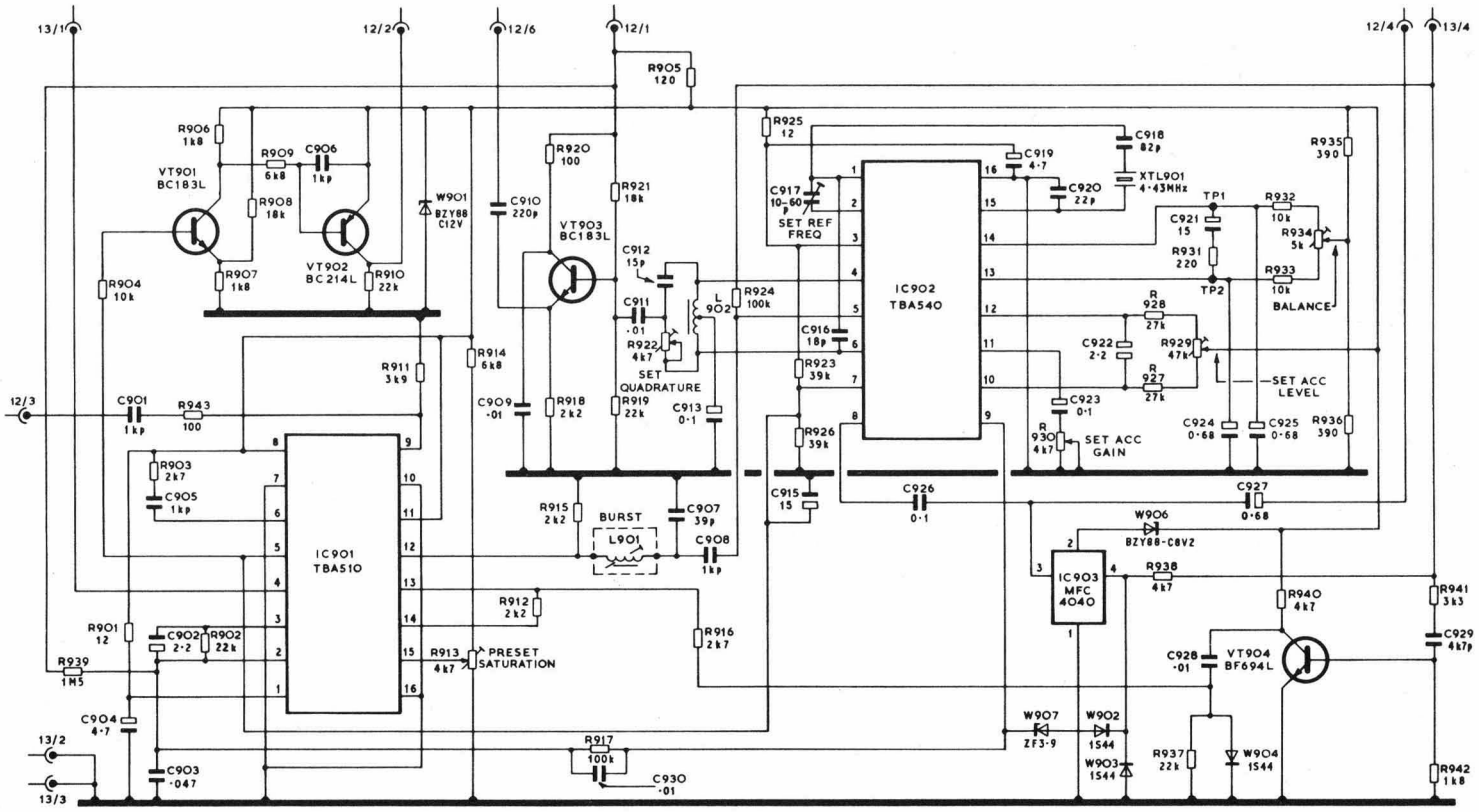


Fig. 5.4



R922 and fed out by emitter follower VT903 at 1.4V pp level. VT901 and VT902 form a switch voltage generator and a trap switch. The input derives from the colour killer line of IC901 pin 5, and the output is connected to the sub-carrier trap on the main signal board. The voltage across R910 will be zero in the absence of colour and 12V with colour present.

Section 6. SOUND IF, DEMODULATION AND OUTPUT CIRCUITS

a. Intercarrier IF and Demodulator

The 4000 series design uses a TBA 120S monolithic integrated circuit IC154 to provide sound IF amplification, limiting, balanced demodulation and audio preamplification with DC gain control, as shown in Fig. 6.1.

Intercarrier signals are obtained from pin 9 of IC101 and passed via R168 to ceramic filter CF151. Because the intercarrier IF is the difference-frequency between sound and vision carriers it will contain unwanted amplitude-modulation from the vision signal and wanted frequency-modulation from the sound signal. The ceramic filter has a well defined bandpass characteristic and will not pass sidebands representing unwanted high frequency vision information. After filtering, the intercarrier signal enters IC154, via pin 14, and passes through eight stages of amplification and limiting to ensure that all remaining amplitude modulation is removed.

Parallel tuned circuit L151 and C166 is fed with a constant amplitude signal from the limiter outputs via pins 6 and 10. In conjunction with capacitors C218 and C219 the tuned circuit gives a 90° phase shift at the nominal unmodulated IF frequency, and greater or lesser phase shifts as the sound carrier frequency is deviated by modulation. The variable phase signal is returned to the IC via pins 7 and 9 to be compared with the unmodified intercarrier signal in a balanced coincidence detector system. The detector output varies proportionally with the change of input frequency so that an audio signal waveform representing the original modulation waveform is recovered.

After demodulation, the audio signal passes through a variable gain preamplifier stage. Volume control R173 operates by changing the DC conditions of this stage, and preset resistor R172 is adjusted so that R173 gives a satisfactory range of adjustment. Following amplification, the audio signal leaves the IC via pin 8 and is subject to a selected degree of treble cut by active tone control circuit R171, C168 and R174 before being passed to the output integrated circuit.

An internal feedback resistor provides negative DC feedback from the output of the eight-stage amplifier limiter to the input via pin 13 and R169. This is necessary to maintain stability as the eight amplifiers are fully DC coupled and have very high open loop gain. An internal zener diode connected to pin 12 is used in conjunction with R167 to provide a stabilised 12V supply on pin 11.

b. Audio Drive and Output Stages (Fig. 6.2)

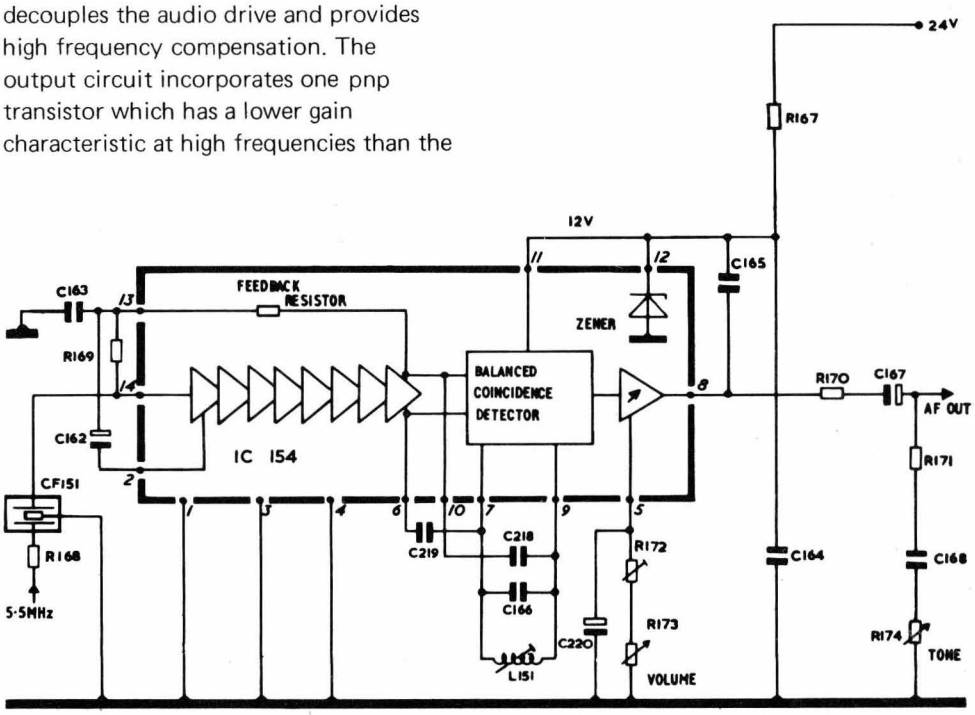
The audio signal from IC154 is applied to the preamplifier section of the drive and output integrated circuit IC153 via pin 1. Resistor R165 provides a half supply voltage which is decoupled by C160 and applied to the input via R166 where it determines the quiescent voltage on output pin 6. Capacitors C157 between pins 1 and 16, and C161 between input and chassis are fitted to decouple very high frequencies.

Audio preamplification in the IC is followed by driver stages and a class B output circuit capable of supplying approximately 3 watts rms to the 16 Ω loudspeaker. C154 from pin 15 to chassis decouples the audio drive and provides high frequency compensation. The output circuit incorporates one pnp transistor which has a lower gain characteristic at high frequencies than the npn devices in the circuit. This is compensated by feedback through C158, which is effectively only on negative output swings, when the pnp transistor is operating.

The principal negative feedback loop is from output pin 6 to the IC preamplifier stages via pin 16. A sample of the output DC quiescent voltage is taken via R164 and R163, but C156 provides a bypass of R163 for AF signals. Shunt components R162 and C155 determine the low frequency roll-off characteristics of the amplifier.

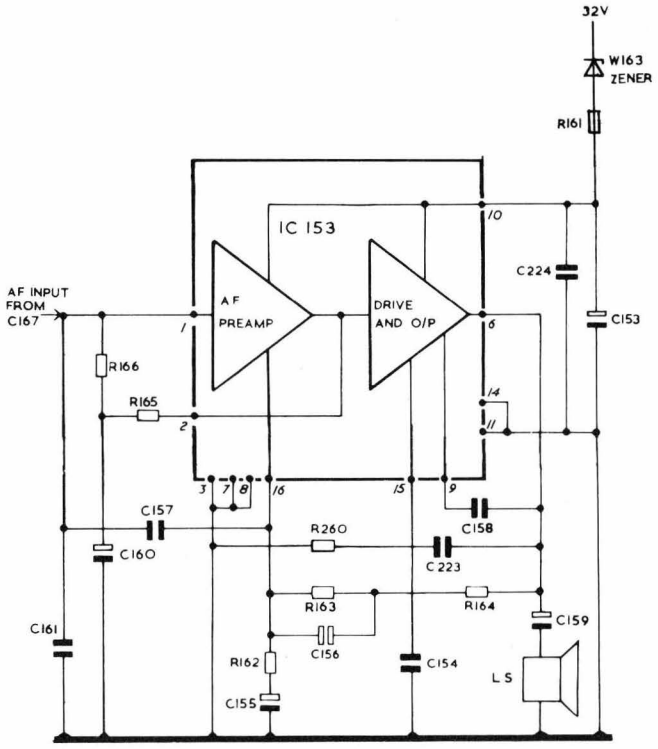
The feedback loop is also used to suppress sound for a few seconds after switch on, thus permitting the tuning and AGC circuits to stabilise on a signal before audio is obtained from the loudspeaker. Before the IC can operate, C155 must be charged to approximately half supply potential, and the values of R163 and R164 ensure that a suitable time delay is achieved. A large value for the loudspeaker coupling capacitor C159 ensures that satisfactory reproduction of low audio frequencies is obtained.

Fig. 6.1



The IC output transistors operate in class B and take heavy currents during loud audio passages. For this reason the circuit is supplied with power from the switched-mode-derived 32V rail, and a decoupled dropping resistor R161 and zener diode W163 reduces this supply to the nominal 28 volts required. It is possible to use a simple dropping arrangement of this type because the IC has a maximum rating of 35V, and thus cannot be damaged under low current and high supply conditions.

A large finned heatsink assembly manufactured from extruded aluminium is incorporated in the IC construction. Centre pins 4, 5, 12 and 13 are omitted and replaced by broad flanges which carry the heat from within the chip and make good thermal and mechanical contact with the main sink assembly. An isolation and matching transformer to permit the use of an extension loudspeaker is available as an optional extra if required.



NOTE PINS 4,5,12 AND 13 NOT FITTED TO IC

Fig. 6.2

Section 7. LINE TIMEBASE AND EHT SYSTEMS

a. Sync Separator, Flywheel, Line Oscillator and Drive Circuits

Notes in Section 3c describe how the switched mode power supply drive is obtained from an integrated circuit IC301. As the oscillator which provides a saw-tooth ramp for switched mode control purposes is locked to line frequency, it is also used as the drive source for the horizontal scanning circuits and EHT generator system. In addition to the many switched mode functions already described, IC301 contains various overload protection systems, as covered in Section 3d; and also a sync separation system; line phase detector and flywheel circuit; oscillator phasing control loop, and output waveform shaping and drive networks. The following notes describe how these sections of the IC together with VT304 operate to provide base drive current for the line and EHT power transistors.

A negative-going vision signal from pin 10 of the IF demodulator IC101 is applied to pin 14 of IC301 via C323 as shown in Fig. 7.1. The leading edge of the sync pulse causes a transistor in the IC to turn-on producing charging current flow out to external capacitor C320 as shown in waveform B of Fig. 7.2. The trailing edge of the sync pulse causes a second transistor to conduct, discharging C320 and thus generating a triangular waveform which is time-displaced relative to the sync pulse as shown.

Field synchronising signals are taken from the lower end of C320 and line pulses go via TF304 and C318 to the flywheel section of the IC via pin 16. In the flywheel circuit the triangular waveform is amplified and clipped to produce a near rectangular pulse which is timed to occur at the centre of the line blanking period. By using this centralised pulse in the flywheel circuit instead of the original sync pulse, a symmetrical oscillator pull-in range is obtained.

The picture displayed on the receiver screen should remain correctly centred and must not be subject to horizontal displacement during the warm-up period. Unfortunately, high voltage line output transistors have an appreciable turn-off delay time and this varies with junction temperature. Commencement of flyback is thus subject to a variable delay which, if uncorrected, would result in horizontal picture position drift.

An efficient flywheel system which compares sync and flyback pulse phase will compensate for drift, but failure of the line output stage could result in the oscillator being uncontrolled and running off-frequency. This would not be satisfactory in the 4000 series because the line oscillator is also providing drive for the switched mode power supply and EHT generator. It is, therefore, necessary to use a comparative waveform which is derived from a fed-back oscillator signal plus an integrated line flyback pulse as shown in Fig. 7.2.

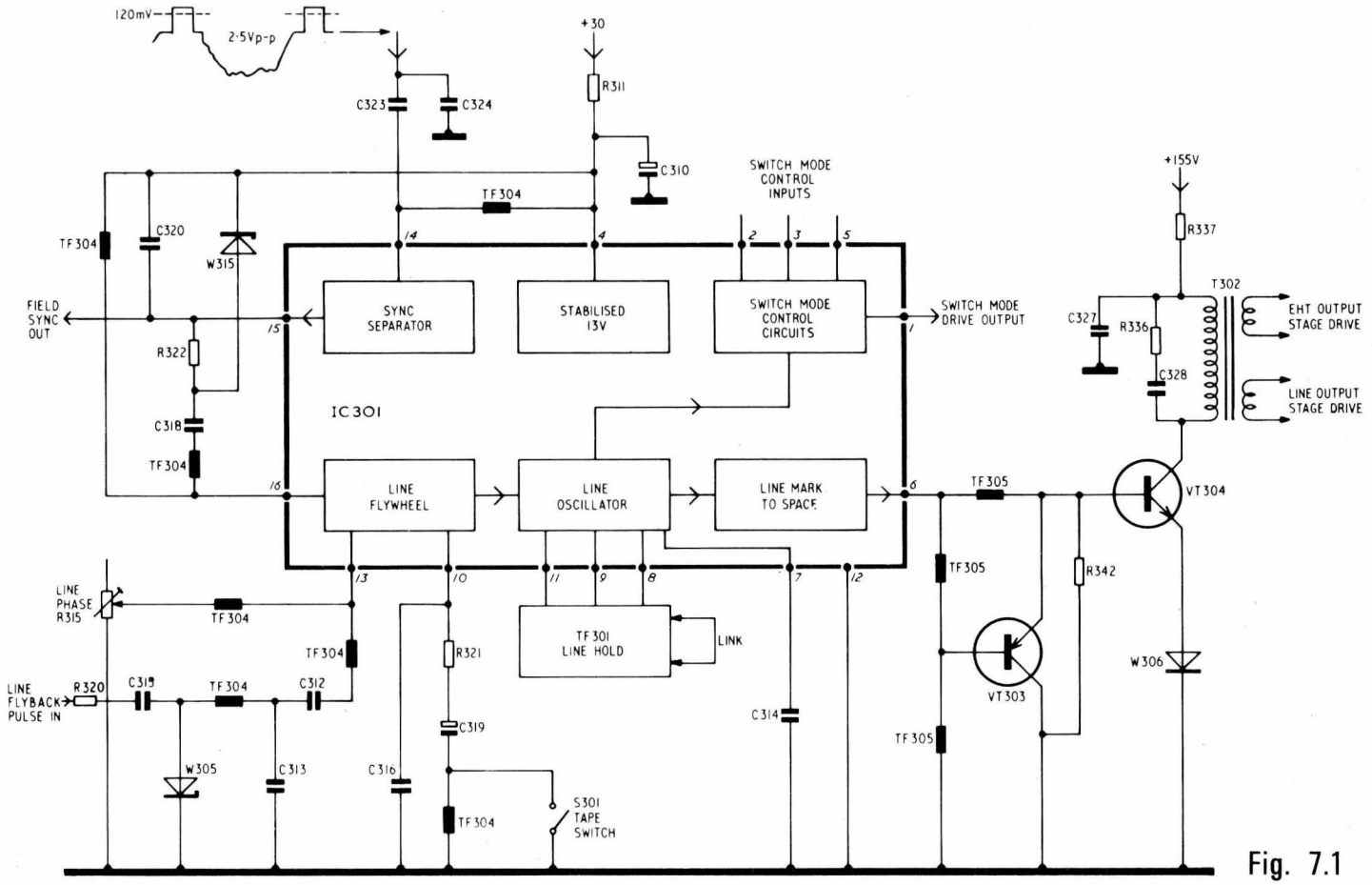


Fig. 7.1

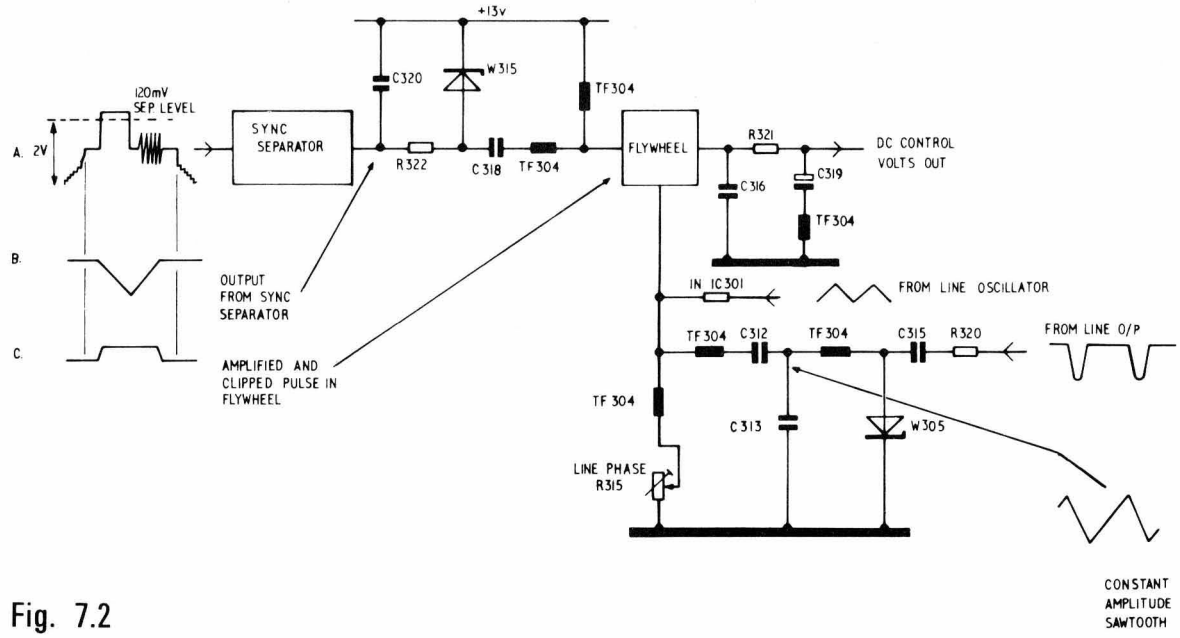


Fig. 7.2

The flyback pulse amplitude varies at field frequency due to east-west pincushion correction as will be described in later Section 7c. Zener diode W305 clips all fed-back pulses at 150V thus removing the modulation and ensuring constant amplitude throughout each field period. Potentiometer R315 supplies a DC bias to pin 13 of the IC via TF304 thus permitting correct adjustment of flyback phase relative to sync and picture information.

The line flywheel time-constant network which consists of C316, C319, R321 and TF304 is connected to pin 10 of IC301. If the receiver is being used with a video cassette or video tape recorder the line phase may fluctuate in a manner not expected with broadcast signals. In these circumstances, a shorter flywheel time-constant is desirable (to permit the line oscillator to follow the signal phase variations) and the tape switch, shown in Fig. 7.1, is opened to add TF304 in series with C319.

The DC control voltage output from the flywheel passes through an emitter follower; and then via IC301 pin 11; and external, special high-stability, thick-film hold control circuit TF301 back to pins 8 and 9 of the oscillator circuit. The thick-film control assembly includes a removable link to give an extended LF oscillator capture range if required. Capacitor C314 forms part of the oscillator tuning circuit and is a special, high stability, silver-mica type.

The oscillator is followed by an amplifier and emitter-follower section which provides low impedance square-wave drive for VT304 via pin 6. The duration of the positive drive waveform at this point is 32μs approximately with a mark-to-space ratio of unity.

The line output and EHT generator transistors both require high base currents to ensure complete saturation during their on periods. This is provided by driver transistor VT304 and transformer T302, which has separate secondary windings for each output stage. VT304 is on when the line output and EHT generator transistors are off, which gives low base-emitter impedances of the latter at high collector voltages.

Driver transistor VT304 is type BD232 and has a comparatively slow turn-off characteristic after saturated operation. To ensure that fast turn-off of VT304 is achieved under all conditions to avoid the risk of over-dissipation, a special base circuit incorporating VT303 is used. When the output from pin 6 of IC301 falls from +12V to near zero, indicating termination of the driver on-period, the minority carriers stored in the base-collector region will tend to maintain the base of VT304 positive with respect to chassis. The base-emitter junction of VT303 is thus forward biased and the transistor will conduct heavily, providing a low impedance discharge path for stored carriers from VT304 base. When the drive from IC301 rises to +12V again, the base of VT303 is held positive with respect to its emitter and the transistor cannot conduct.

Silicon diode W306 in VT304 emitter circuit provides a bias of approximately 0.6V during transistor conduction. Dropping resistor R337, decoupled by C327 reduces the supply rail to approximately 130V before application to VT304 collector via T302. Damping network R336 and C328 provides protection for VT304 by absorbing voltage spikes which arise due to the inductance of T302 primary winding.

b. Line Output Stage and East-West Pincushion Correction

The line output transistor VT305 in Fig. 7.3. is type BU208 which has a collector-emitter rating of 1500V and can pass 5A peak current. Because of their physical construction, high voltage transistors usually have slow turn-off characteristics and the BU208 can take up to 10μs to change from a saturated to a non-conductive state. It is essential that the line output transistor collector current does not tail off slowly as this would result in high dissipation and reduced device reliability.

During its on-period the transistor must be fully saturated and device spreads require that adequate base current is available to suit bottom limit devices, so that nominal transistors are usually overdriven to some extent. As the end of scan approaches, the positive-drive waveform from T302 is terminated, but inductor L304 maintains base current which slowly falls from its original

overdrive level. After a few microseconds, the transistor comes out of saturation, but as the drive has been progressively reduced there is a minimal amount of stored charge carriers in the semiconductor and rapid turn-off occurs.

The line windings on the deflection toroid L306 and L307 are series connected and have an inductance of 1.25mH, a resistance of 1.7Ω, and require approximately 6A pp for full scanning at 25kV. Pulse voltage between line and field windings on the toroid must not exceed 700V and a balanced arrangement with inductor T303 distributes the 1200V flyback pulse as a 600V positive pulse at VT305 collector and a 600V negative pulse at the emitter. This balanced arrangement also helps to minimise electromagnetic radiation from the deflection assembly.

Capacitor C371 provides an energy reservoir for the scanning cycle and also gives the required degree of 'S' correction. C331 (part flyback tunng) is connected directly across the output transistor to provide a degree of protection from voltage spikes under flashover conditions. Line linearity reactor L371 is effective during the first third of scan to cover the transition period between transistor action inversion, i.e. collector-base conduction and normal transistor action in VT305, after which it becomes magnetically saturated and has very low impedance.

Horizontal picture shift is obtained by shunting a small fraction of the scanning current through L372 and W371. As current can only pass in one direction through W371, a DC component flows around this circuit and through scan coil windings L306 and L307, giving a horizontal picture displacement. The shift adjustment controls R372 the effectiveness of W371 by providing shunt impendances varying between short-circuit and 500Ω. A switch S371 is provided to reverse W371 giving picture shift in the opposite direction if required.

The primary function of inductor T303 is to ensure equal and opposite flyback pulses at VT305 collector and emitter as previously explained, but the assembly also has additional windings to supply line frequency pulses to other sections of the receiver. A small coupling coil on T303 feeds a circuit, containing L303 and C330, which is connected to the 32V switched mode derived supply via a thick-film balanced resistor network TF307. L303 simulates the inductance of line deflector coils and a sawtooth current is obtained between the points shown in Fig. 7.3. Capacitor C330 simulates the conventional 'S' correction component and a parabolic voltage is extracted. These waveforms are used by the convergence circuitry. The inductor T303 has further windings with an earthed centre-tap and thus provides flyback pulses of both polarities to drive circuits in various parts of the receiver.

With 110° tubes, geometrical factors result in a higher degree of pincushion distortion which must be corrected by modulation of the scanning waveforms. In the 4000 design, a thick-film assembly designated TF302 provides much of the E–W pincushion circuitry and contains components shown in the lower-left section of Fig 7.3 without reference numbers. Components not incorporated in the assembly include variable resistors R344, R345, R346 and power transistor VT306.

A tilted parabolic field-frequency waveform is applied to the top of E–W pincushion amp. control R346 through C333 and then via R_3 (2.7kΩ resistor) to the base of VT_1 type BC182L. A negative-going field-frequency sawtooth is applied to the E–W pincushion tilt control R345, as shown, and passes via R_5 to VT_1 emitter. Because the waveforms are applied to base and emitter respectively, subtraction takes place and the 'amp' and 'tilt' control can be adjusted to produce a symmetrical parabola or one with a tilt in either direction across collector load, R_1.

VT_2 operates as a driver for VT306 which is a power device carrying the supply current of the line output transistor. Reference to Fig. 7.3. shows that the positive-going parabola waveform becomes negative-going after the tilt-subtraction stage, positive-going after VT_2 and negative-going at VT306 collector. VT306 is passing maximum current and has minimum collector voltage at a point half-way through the field scan cycle, and picture width is progressively increased during the first half of field scan and progressively decreased during the second half. Line scanning is thus modulated with a 'barrel' characteristic which compensates for E–W pincushion distortion in the picture tube.

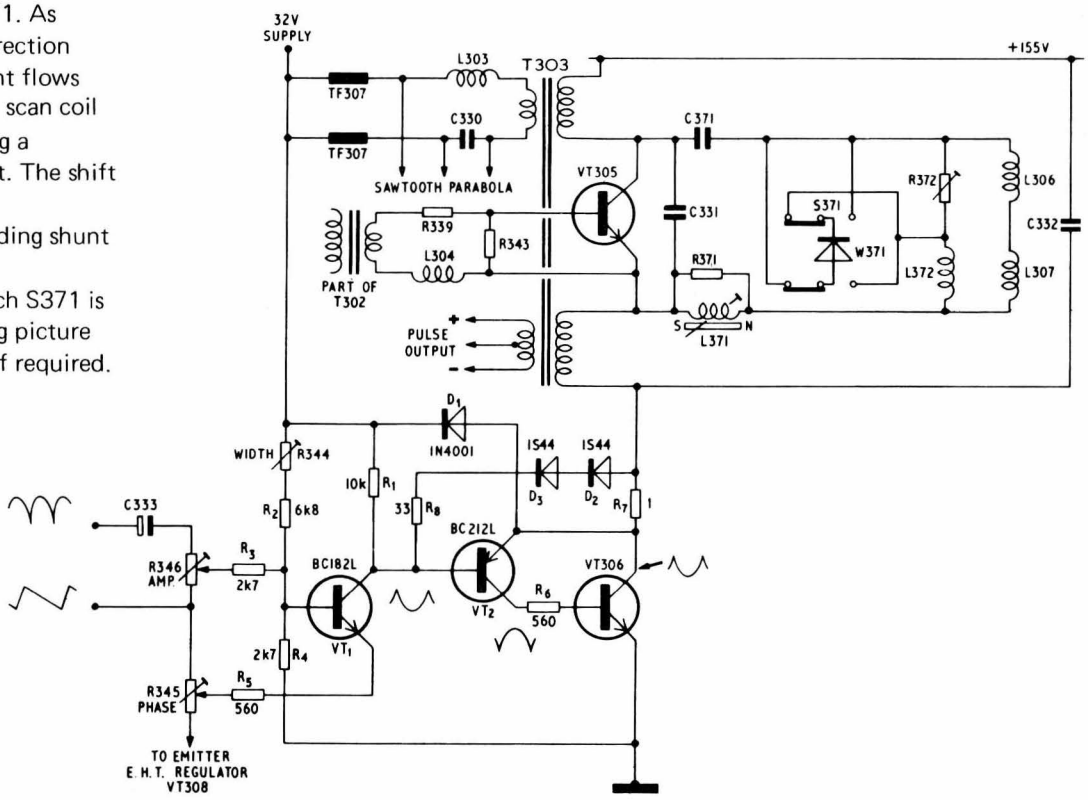


Fig. 7.3

Base bias in VT_1 is controlled by variable resistor R344, which, because of the DC coupling, controls the mean current through VT306 and the line output transistor VT305, thus giving a picture width adjustment. Automatic width adjustment is provided by a connection between the EHT regulator transistor VT308 emitter and the lower end of R345 as shown. If the EHT voltage falls due to increased loading, the emitter of VT308 becomes more positive and this causes the emitter of VT_1 also to become more positive with respect to the base.Current through VT306 falls and collecter voltage rises leaving a lower operating voltage for the line output transistor and reducing width to compensate for the fall in EHT.

The three diodes in the circuit are included to protect VT306 from damage in the event of a collector-to-emitter short-circuit of line output transistor VT305. Excessive voltage drop across R_7 will cause both D_2 and D_3 diodes to conduct, turning off VT_2 and removing drive from VT306. Line output current supply can now flow via D_1 to the 32V supply rail and the overvoltage trip will be fired turning off the receiver.

c. EHT Generator Stage

The EHT generator transistor VT307 is type BU126 which has a fast turn-off characteristic, can pass currents of 3A, and operate with up to 750V between collector and emitter. Base drive for VT307 is obtained from a secondary winding on T302 as shown in Fig. 7.4 with R338 to limit base current and provide stabilisation against changes in Vbe. The EHT transformer T305 is fed from the 155V rail via choke L305 and decoupled through C334. Effectively across the primary winding of T305, C335 tunes the transformer to give a half-line period pulse-duration of 26μs.

The windings of T305 (see Fig. 7.4.) develop an 8.5kV pulse to drive the EHT tripler unit. Rectifier W308 is fed from a suitable tapping point and develops 1.2kV DC to feed the CRT A1 electrode potentiometers. The tripler unit is a conventional Cockcroft-Walton circuit using silicon diodes and wound capacitors. Focus voltage is obtained from the first stage which supplies 8.5kV DC to a special, high-stability, thick-film potentiometer assembly.

The voltage drop across R349, in the emitter of VT308, will vary in proportion to the EHT loading and is taken via the variable resistor R348 to provide beam limiter control bias for IC155 as described in Section 5c. Circuits in TF303 drive VT308 to obtain automatic width stabilisation with varying EHT as already described in Section 7b.

VT308 and TF303 control the emitter voltage of VT307 by sensing the A1 voltage via R352. VT308 acts as a series regulator controlling the voltage available to the EHT generator, increasing the feed if A1 voltage drops and vice versa. The effective internal impedance of the EHT is thus maintained less than IMΩ over the entire working range.

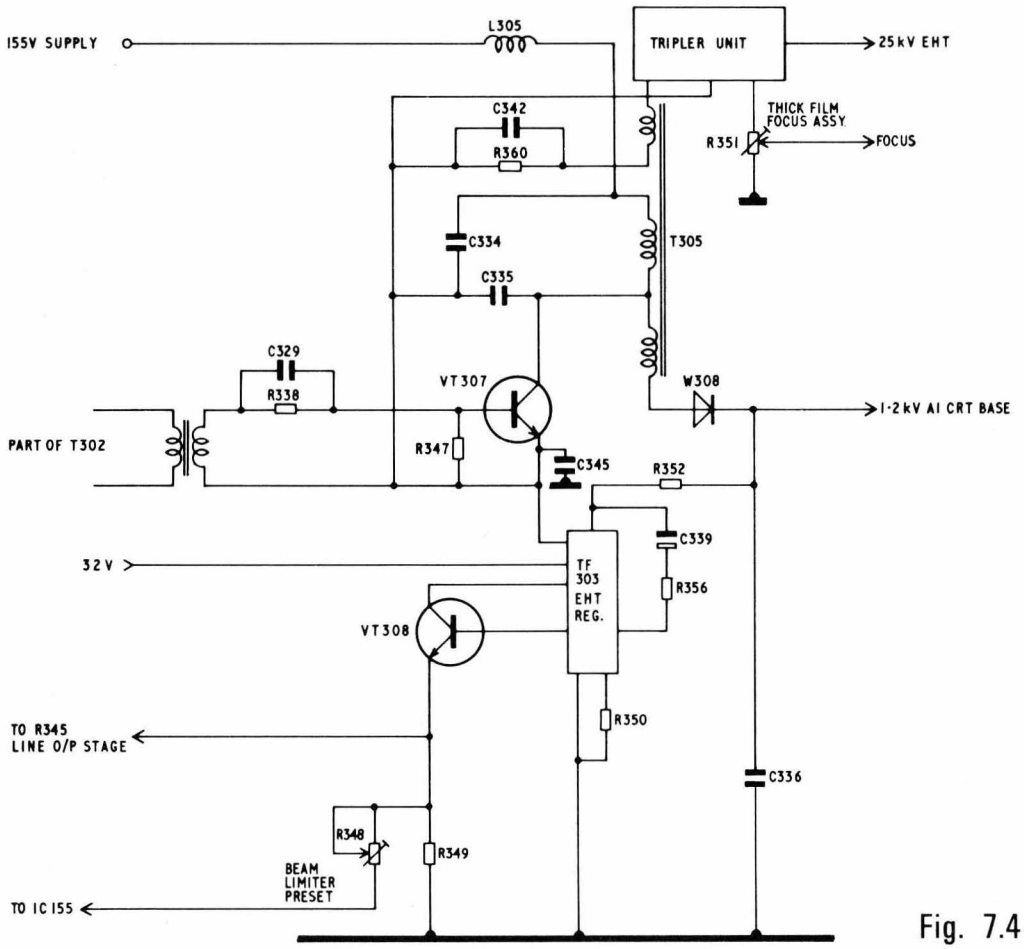
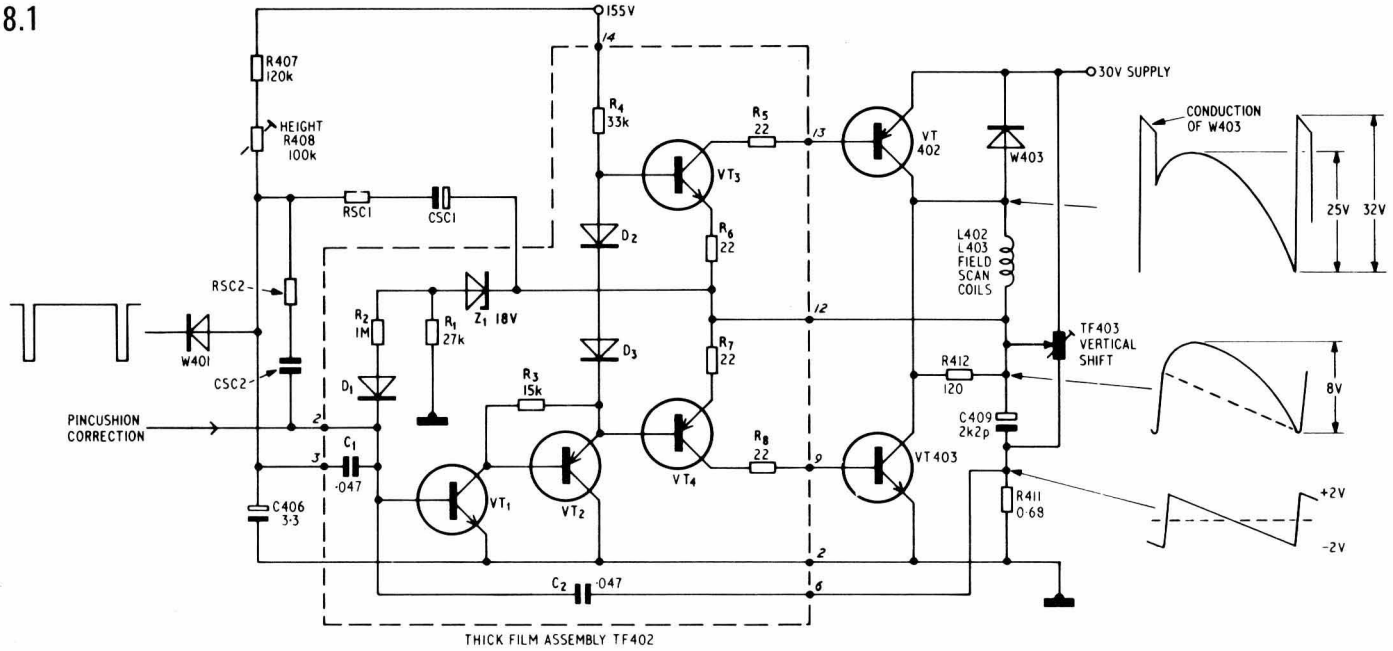


Fig. 7.4

Section 8. FIELD TIMEBASE

Fig. 8.1



a. Field Oscillator (Fig. 8.1)

The field oscillator is a multivibrator circuit and forms part of thick-film assembly TF401. Negative-going sync pulses from pin 15 of IC301 are integrated by R_2 and C_1. The sync level at pin 2 is at +12V between the field sync pulses and is built up through integration during the field pulse period to about 18V at the anode of D_1. When the field sync pulse train occurs the cathode of D_1 falls to approximately 10V which causes the diode to conduct, reducing current in VT_1, and initiating turn-off and flyback.

During flyback, the base of VT_1 is negative with respect to chassis so that D_1 is now heavily reverse biased, preventing random pulses or noise from the sync separator having any effect on flyback duration and interlace. Flyback is normally completed in 0.7ms to 1ms and the voltage at W401 cathode swings between 30V and near chassis potential as shown. Diodes D_2 and D_3 protect the transistor base-emitter junctions against excess reverse voltage.

b. Sawtooth Generator, Driver and Output Circuits (Fig. 8.2)

The field scan amplifier consists of preamplifier and driver sections incorporated in thick-film assembly TF402, followed by complementary power output transistors VT402 and VT403.

Transistors VT_1 and VT_2 operate as a complementary Darlington circuit which gives the usual high current gain of a conventional Darlington arrangement, but has only one base-emitter junction across

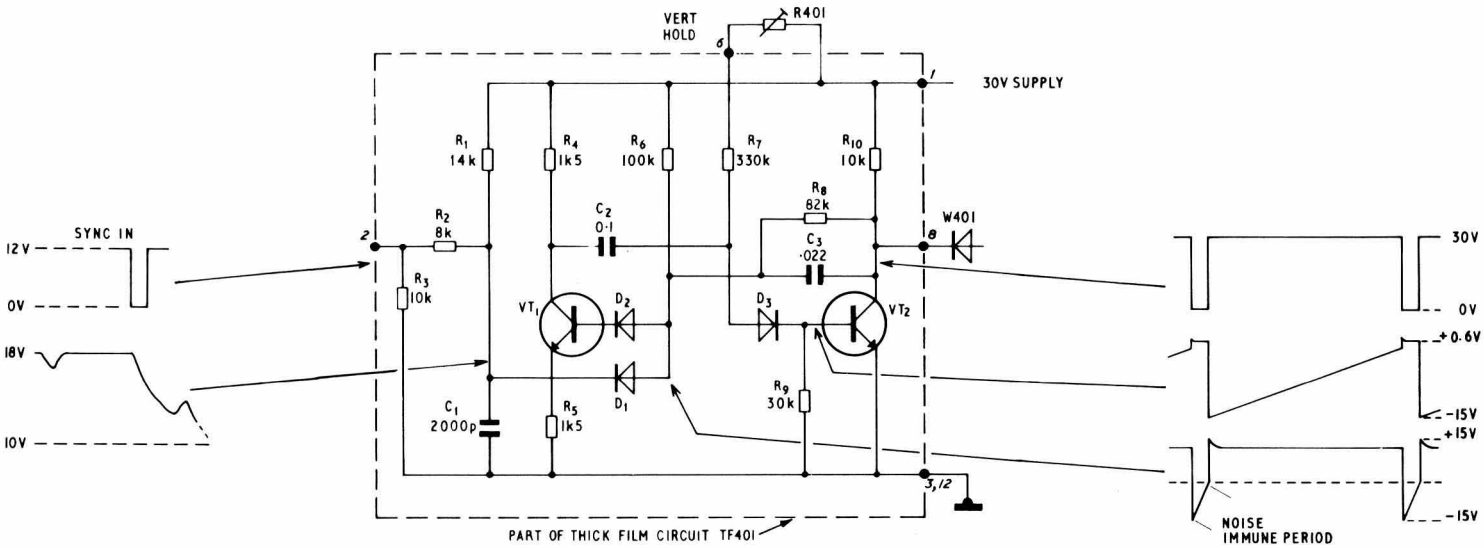


Fig. 8.2

the input which can contribute to thermal drift. Driver transistors VT_3 and VT_4 are fed with base bias from the 155V supply via a 33kΩ resistor R_4 which also provides the load for VT_2.

The driver and output transistors are operated in class B and diodes D_2 and D_3 provide a small, temperature-compensated, forward bias which minimises crossover distortion.

VT402 and VT403 are complementary power transistors mounted on a substantial heatsink assembly and together provide a current of nearly 6A pp through the field scan coils L402, L403.

During the first part of field scan, VT402 conducts and passes a progressively reducing current from the supply through the deflection windings to charge C409. During the second half of scan, VT403 conducts allowing C409 to discharge at a progressively increasing rate through the deflection coils. Scanning current in both directions also passes through 0.68Ω feedback-sensing resistor R411 and produces a negative-going sawtooth voltage as shown in Fig. 8.2.
The voltage across R411 is taken via C_2 to the preamplifier stage input, providing a high degree of current-derived negative feedback. This has many beneficial effects on amplifier operation including open- and short-circuit load protection for the output transistors; elimination of non-linearities, such as crossover effects, which may occur in the amplifier circuit; and removal of variations in linearity and height due to capacity changes in C409, or resistance changes in the deflection windings.

Drive for the preamplifier is provided by a positive-going sawtooth voltage across C406. At the completion of flyback C406 begins to charge up towards the 155V line via R407 and Height control R408. During the field forward-scan period, C406 will charge to only a small percentage of the aiming voltage, and a very linear ramp waveform is generated. When sync pulses occur, the multivibrator oscillator is triggered and W401 cathode falls to near chassis potential providing a low resistance discharge path for C406.

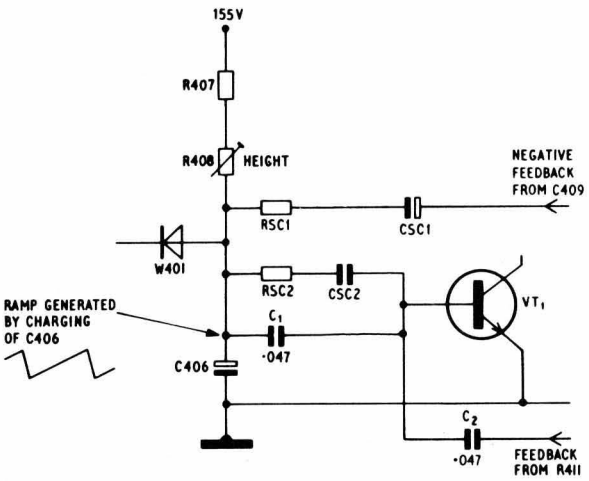
Waveforms present across the various output circuit components are shown in Fig. 8.2. The negative-going sawtooth across R411 has an amplitude of approximately 4V pp. Sawtooth current flow into and out of C409 produces a parabolic voltage across the capacitor which, when measured relative to chassis, will also include the sawtooth waveform due to R411 as shown. When field flyback takes place, the collectors of VT402 and VT403 change rapidly from near chassis potential to just below 30V, and the deflection winding inductance causes a large positive flyback pulse to occur. As the pulse swings above 30V, W403 becomes forward biased and current flows into the supply rail, limiting the amplitude to approximately 32V.

D_1, together with the input capacity of VT_1, forms a peak detector circuit to provide a bias which is DC coupled via VT_1, VT_2, VT_3 and VT_4 to define the output pair centre-point at about 15V. Vertical picture positioning is adjusted by TF403 which is a special thick-film assembly incorporating individual high wattage resistor elements selected by a make-before-break rotary switch. A high-wattage requirement is necessary because the low field deflection sensitivity of 110° scanning toroids makes it necessary to use fairly large currents for shift purposes. TF403 is connected between the 30V supply rail and R411, and adjustments of the slider will result in current flowing through scan coils L402 and L403 to or from the 15V centre-point of VT402 and VT403.

The excellent linearity of the sawtooth ramp input together with the minimal distortion in the drive and output circuitry (due to current-derived negative feedback) ensure good field linearity. The current waveform through the deflection windings must contain a small degree of 'S' curvature, however, to correct for distortion in the picture tube due to variations in distance between deflection-centres and faceplate over the scanning cycle. Components RSC1, RSC2, CSC1 and CSC2 which provide 'S' correction are included in Fig. 8.2 but are repeated in Fig. 8.3 together with relevant waveforms.

c. Field 'S' Correction (Fig. 8.3)

VT_1 has a significant input capacitance (due to the Miller effect of C_2 from R411) which, together with RSC2, produces an integrating action and modifies the linear ramp as shown by waveform B. A tilted parabolic waveform from the top of C409 is also applied via CSC1 and RSC1 as negative feedback which subtracts from the ramp across C406. The cancellation effect is greatest towards the end of scan where the tilted parabola voltage is falling rapidly and this modifies the integrated input signal as shown in waveform C. Current flow in the deflection coils is thus correctly modulated as shown in waveform D to compensate for the effects of picture tube geometry.



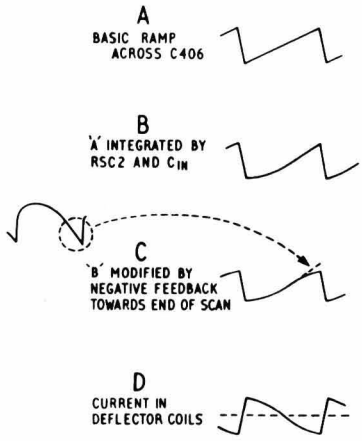


Fig. 8.3

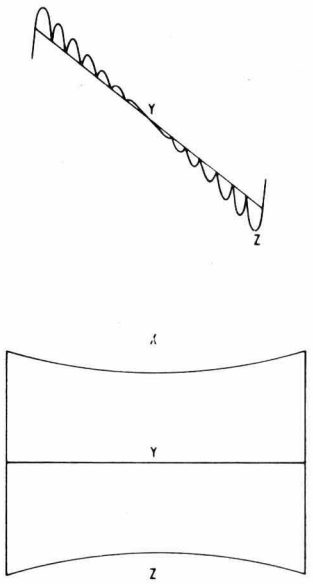


Fig. 8.4

d. North-South Pincushion Correction and Blanking (Fig. 8.4, 8.5, and 8.6)

Geometrical factors result in a considerable degree of pincushion distortion with 110° tubes and this must be compensated by modulating the scanning currents so that a straight-sided picture is obtained. Curvature at the top and bottom of the raster can only be corrected by a variation of vertical scanning current at line rate. Fig. 8.4 illustrates a current sawtooth representing one field sweep with an associated raster below.

Fig. 8.5 gives a simplified illustration of the circuit incorporating VT401 which produces line pulses varying in amplitude and polarity as required. The transistor collector is returned to chassis through R405, and the emitter is supplied with field-frequency sawtooth voltage from across R411. R411 carries the deflection current as explained in previous Section 8b. The transistor base is supplied with a large amplitude positive-going line flyback pulse via 1kΩ resistor R403.

During the second half of scan, the emitter of VT401 is made progressively more negative with respect to collector by the field sawtooth 'V' as shown in Fig. 8.5A, and the transistor will thus be correctly biased for normal operation when the large amplitude line pulse forward biases the base-emitter junction. Whilst the line pulse is applied, complete saturation occurs making the transistor virtually short-circuit, so that the falling sawtooth negative emitter voltage 'V' appears at the collector in the form of rectangular pulses at line rate, as shown.

Operation of the circuit during the first half of field scan is illustrated in Fig. 8.5B. The emitter of VT401 now has a falling voltage applied which is positive with respect to the collector and this is the wrong polarity for normal operation. The transistor collector and emitter regions both consist of n-type semiconductor, however, and the usual bias polarities are reversed. The junctions change roles, with the emitter becoming the collector and collector becoming emitter. Line gating pulses take the base positive with respect to the acting emitter and saturation occurs. This results in the falling positive field sawtooth voltage 'W' appearing at the output in the form of rectangular line rate pulses, as shown.

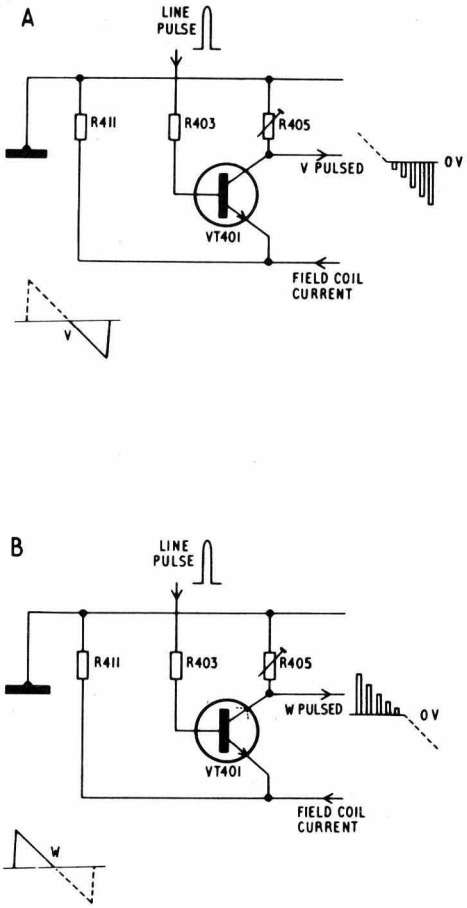


Fig. 8.5

Complete N-S pincushion-correction circuitry is shown in Fig. 8.6. VT_3 operates as a Miller integrator due to R_{14} and capacitive feedback from collector to base via C_4. This results in a near parabolic line waveform being developed across the collector load resistor R_{15}. N-S pin. phase control R402 provides a final and adjustable degree of integration in conjunction with the main amplifier

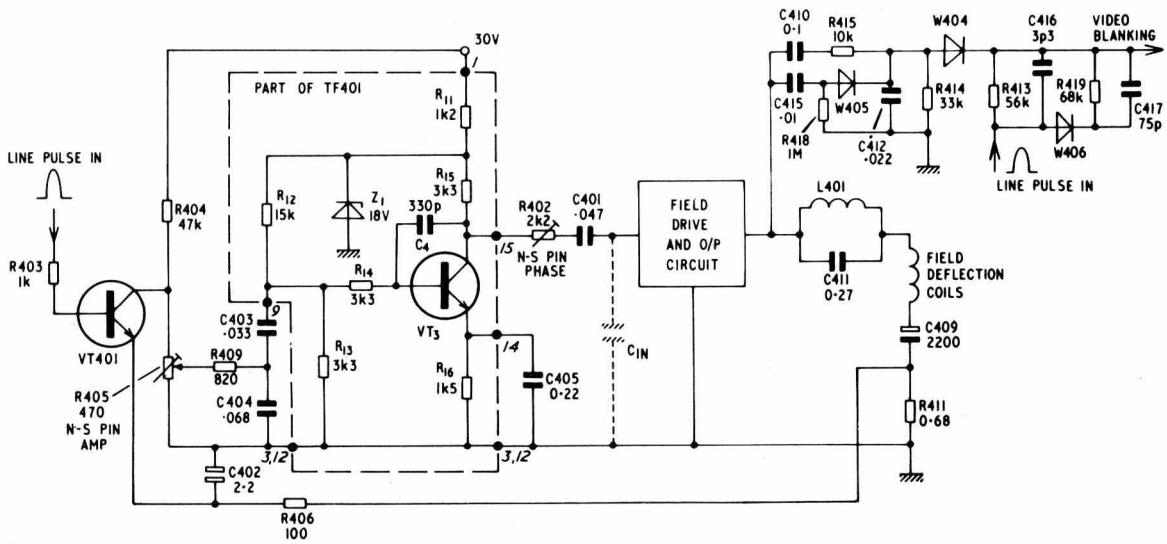


Fig. 8.6

input capacitance so that a symmetrical line parabola is added to the 'S' corrected field waveform at the preamplifier input as shown in Fig. 8.2.

Parallel tuned circuit L401, C411 (Fig. 8.6) is resonant at approximately 1kHz and thus has very low impedance at the field scanning frequency of 50Hz. At frequencies above resonance the circuit exhibits capacitive reactance which resonates with the deflection coil inductance to form an acceptor circuit tuned to line frequency at 15.625kHz. By this means it is possible to produce the large amplitude line frequency currents required in the field coils from the same voltage drive source as used for field frequencies, despite the much increased inductive reactance.

The field flyback pulse is used to provide a blanking signal for application to IC157. C415, W405 and R418 serve to sharpen the leading edge of the field blanking pulse. Line blanking pulses are injected via R413, as shown, and W404 serves to isolate these from the low-pass filter circuit and also to protect the IC input transistor against excessive reverse bias due to negative excursions of the field waveform across C412. The leading edge of the blanking pulse is speeded up by the differentiating action of C417 and R419. W406 prevents the trailing edge of the pulse from being affected. C416 shifts the whole pulse into the correct position.

Section 9. CONVERGENCE

a. General Description of Convergence System

The 4000 series convergence system is housed in two assemblies, a hand-held unit which accommodates waveform shaping circuits and all static and dynamic controls; and a CRT neck unit which includes active convergence drive circuits and associated coil and pole piece assemblies. Fig. 9.1 illustrates the sequence of low level shaping and control circuitry for line- and field-derived waveforms, the power drive sections which feed combined signals to individual gun pole pieces, and the DC static convergence control systems.

The hand-held unit contains twelve low wattage carbon potentiometers (10kΩ each) providing all dynamic convergence adjustments and four purpose-designed thick-film assemblies giving control of radial and lateral static convergence by variation of current through the large coils on the appropriate pole pieces. Line-derived sawtooth and parabolic waveforms are passed through control potentiometers at low level without additional shaping or amplification. The field-derived waveform is processed by two active circuits on a thick-film assembly giving independent convergence adjustments in the top and bottom picture areas.

The neck unit is built around a precision deflection toroid and incorporates large area heatsinks for the three principal convergence power transistors which drive current through the small R, G and B pole piece coils as shown. The neck unit incorporates two thick-film assemblies. The first provides preamplification, matrix circuitry and bias systems for the red and green power transistors. The second contains preamplification and bias circuits for the blue power transistor (which handles the line frequency and fixed amplitude field frequency currents) plus an additional low power amplifier supplying variable amplitude field frequency waveforms which are added to the blue static convergence current as shown.

b. Static Convergence Circuits

All three radial static convergence adjustments are made by operating potentiometers on the hand-held unit. These control currents through the pair of large coils on each pole piece assembly to provide a variable magnetic field in either direction as required. The convergence assembly does not incorporate permanent magnets.

The radial static convergence circuit is illustrated in Fig. 9.2A. A potential divider across the 32V supply, consisting of two, 800Ω resistors in the red and green circuits, and 200Ω resistors in the blue circuit, provides two arms of a bridge circuit to which one end of the large convergence coil is returned. The shift controls in the hand-held unit are specially designed thick-film potentiometers and have low resistance high wattage rating at the track ends tapering to a high resistance low wattage rating in the centres as shown

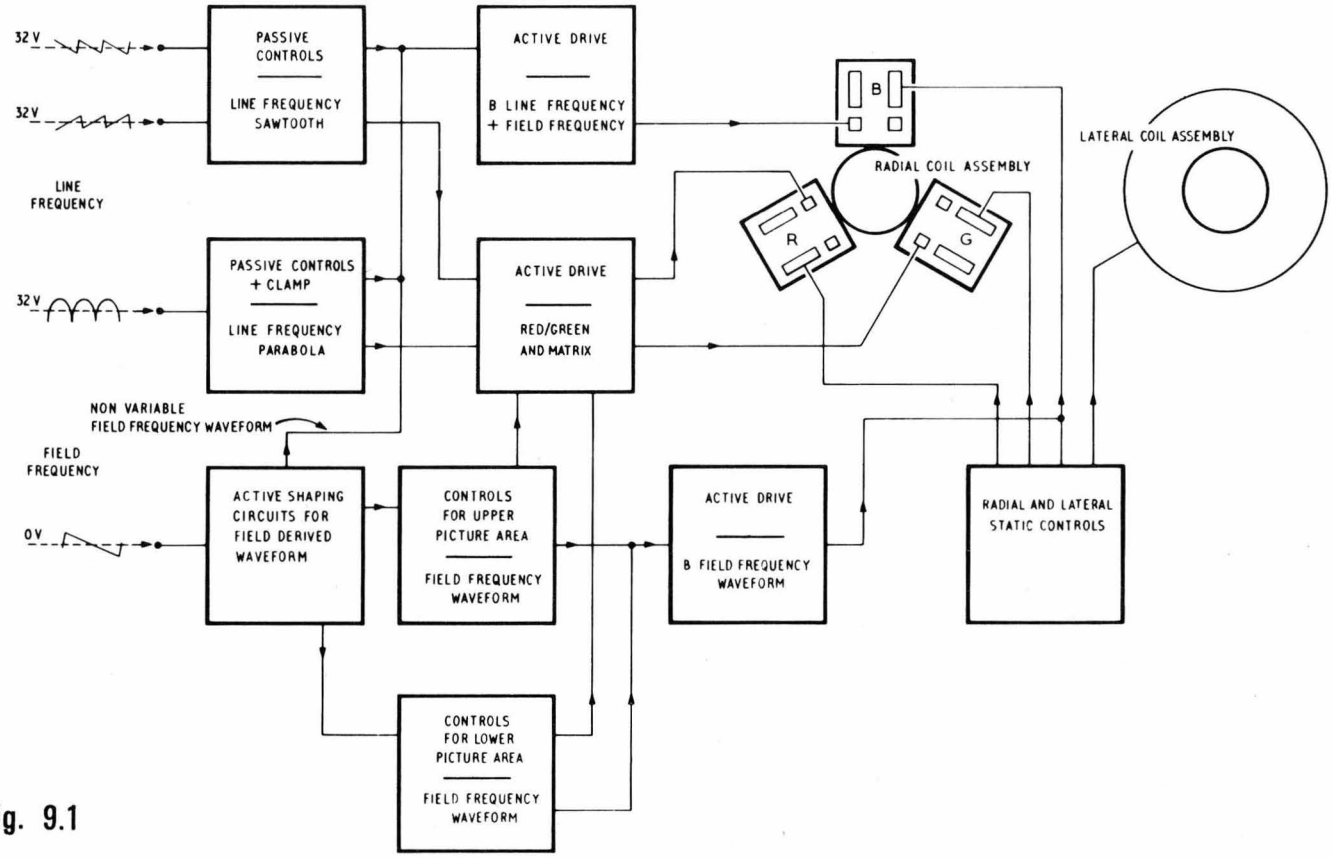
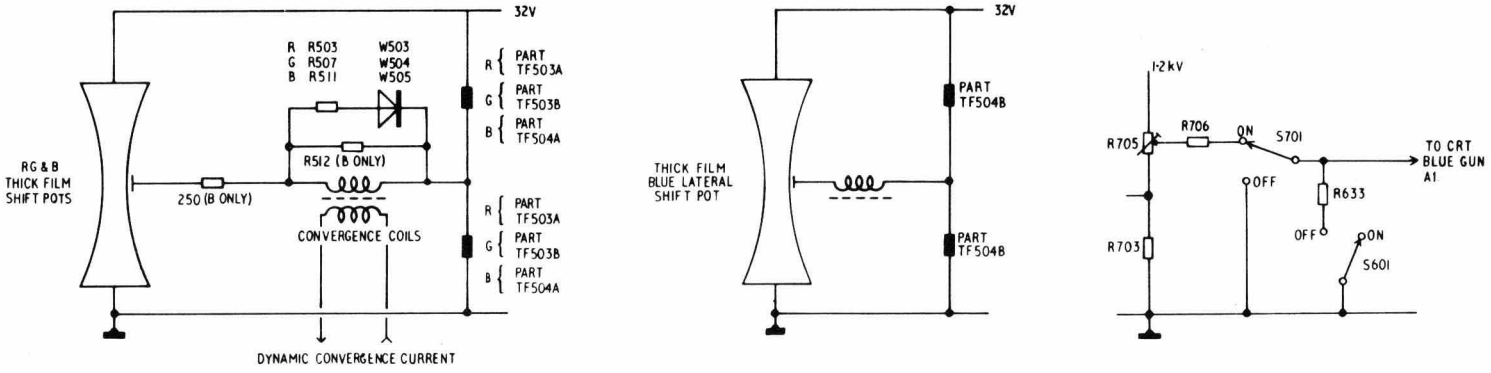


Fig. 9.1



A B C

Fig. 9.2

symbolically in the diagram. When a slider is central it will balance the bridge and no current will pass through the slider contact or convergence coil. Under this condition there will be only bleed current through the potentiometer and dissipation will be at a minimum. As the slider is moved away from the centre there will be an increasing current flow through the convergence coil-slider circuit and the end portion of the track will operate at increased wattage dissipation.

The large coils used for static convergence are mounted on the pole pieces adjacent to smaller coils carrying dynamic convergence currents. Transformer action results in the variable amplitude dynamic waveforms appearing in the static circuit and DC clamping is necessary to prevent changes in centre convergence as the dynamic controls are adjusted.

The blue lateral static convergence circuit is shown in Fig. 9.2B. Operation is similar to the R, G and B radial static circuits. Convergence set-up is facilitated if the blue raster is temporarily extinguished whilst the red and green rasters are converged. For this purpose the hand-held unit includes a switch for blue gun suppression as shown in Fig. 9.2C. R, G and B gun switches (S701, S702, S703) are also provided on the CRT base assembly for use during servicing and general set-up adjustments.

c. Waveform Shaping and Control Circuits

Line frequency parabola and tilt convergence waveforms are obtained from the shaping circuit associated with T303 in the line output stage. A parabolic voltage developed across C330 is fed via C601 to three paralleled 10kΩ controls (R612, R614, R616) as shown in Fig. 9.3. A sawtooth voltage developed across TF307 in the line output stage, is applied directly across three paralleled 10kΩ controls (R604, R605, R606) to provide an adjustable line frequency tilt component. The waveform is symmetrical in amplitude about the 32V supply and when added at low amplitude to the clamped parabolic signal will not result in a variation of DC level.

The field-frequency sawtooth across R411 in the vertical scan output circuit is fed to thick-film assembly TF601 in the hand-held unit, where it is applied to transistors VT_1 and VT_2 as shown in Fig. 9.4. The amplitude of this waveform is approximately 4V pp and it has been divided into five sections with six selected voltage levels as shown.

At the start of field scan the input sawtooth is at +2V and VT_2 base will be forward biased giving a collector current which produces a positive voltage across the emitter resistor R_6 large enough to turn on VT_3. As the input waveform falls from +2V, the collector current of both transistors will fall resulting in a rising voltage at the lower end of the three parallel-connected controls R626, R628, R630. When the input sawtooth reaches about 1.2V (2 x Vbe) the voltage across VT_2 emitter resistor R_6 will be approximately 0.6V causing VT_3 to turn off. The falling input waveform is now only controlling current in VT_2 and the rate of collector voltage rise is reduced. When the input drops below 0.6V (Vbe) VT_2 turns off also. As the input sawtooth passes through zero the emitter becomes negative; and VT_1, which is a Miller integrator stage, turns on and the emitter input voltage appears at the collector in an amplified and integrated form. Stage gain is controlled by C602 and the value of R_3. Resistors and diodes in the base circuit of VT_1 serve the purpose of obtaining the negative waveform at the collector of VT_1.

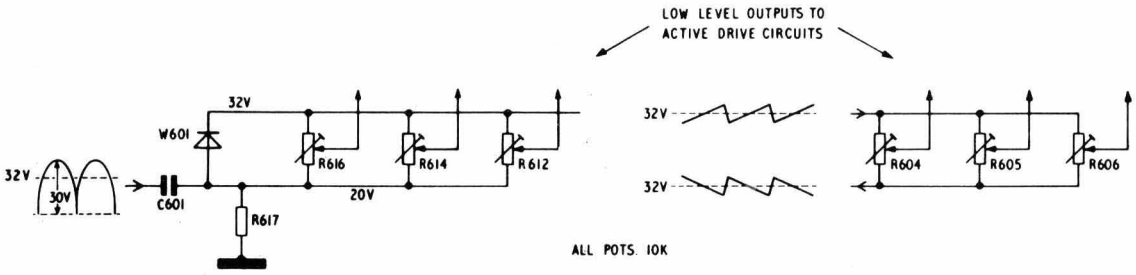
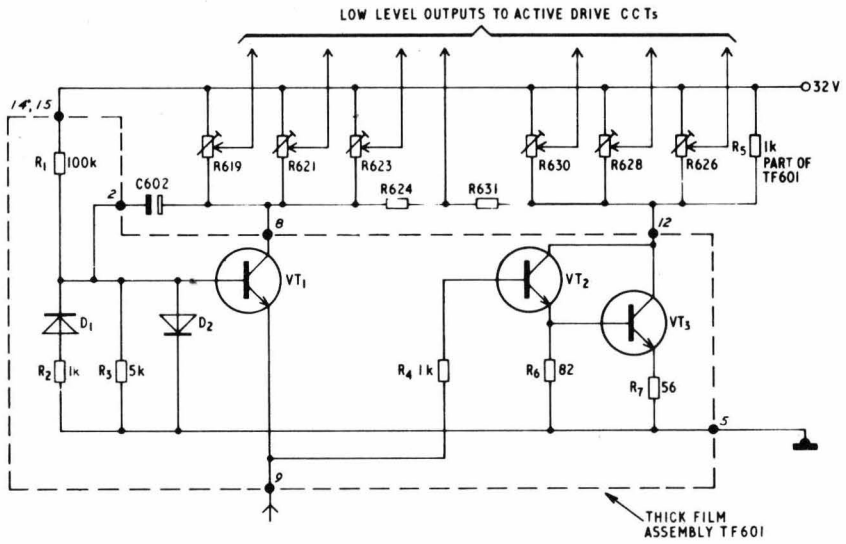


Fig. 9.3



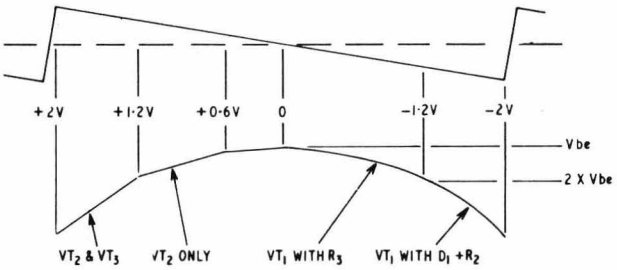


Fig. 9.4

The three potentiometers R619, R621, R623 in Fig. 9.4 control the voltage waveforms for the convergence adjustment produced during the second half of field scan and will thus have effect in the lower half of the picture. Correspondingly, the potentiometers R626, R628, R630 control waveforms derived during the first part of scan and will affect convergence in the upper picture areas. Resistors R624 and R631 produce a non-adjustable combined waveform which is added to adjustable line frequency waveforms before being fed to the blue power output stage.

d. Red-Green Matrix and Drive Circuit

Line and field derived convergence waveforms are fed at low level to the CRT neck unit which accommodates an RG matrix circuit and power transistors to provide current drive for the convergence coils. A simplified diagram of the matrix circuit is given in Fig. 9.5. The lower transistors VT501 and VT502 are power types. VT_1 and VT_2 are small signal high gain transistors and their emitter current is not significant in determining the voltages at 'X' and 'Y'. The matrix and drive circuit normally handles a mixture of DC restored 50Hz and 15.625kHz signals plus harmonics.

The bias and feedback systems of the VT_1 and VT_2 amplifier stages are so arranged, that an input signal at point 'H' generates identical current changes in the same direction (both increasing or decreasing) in the red and green convergence coils; thus picture elements of the red and green rasters shift horizontally with respect to each other. An input signal at point 'V' causes the same currents, but in mutually opposite directions, to flow through the convergence coils; thus horizontal red and green raster-lines mutually shift in a vertical direction.

The complete RG matrix and drive circuit is illustrated on the left of Fig. 9.6. All components except power output transistors VT501, VT502 and the convergence windings are incorporated in a single thick-film assembly TF501.

The line- and field-derived waveforms from the hand-held unit are DC clamped to the 32V line. To make a direct coupling to the VT_1 and VT_2 bases possible, diodes D_1 and D_2 are fitted and fed from their own voltage divider (R5, R6, R7, R8) placed between the 40.2V and 20V lines. Thus the diodes remain always conducting without loading the control circuits.

e. Blue Drive Circuits (right side of Fig. 9.6)

The main blue drive circuit handles adjustable amplitude line frequency signals and a fixed amplitude field-frequency signal. These are fed to the B line-frequency input terminal (pin 1) from the hand-held unit and pass via voltage compensation diode D_1 and amplifier transistor VT_1 to power driver stage VT503. The collector current of VT503 flows through the small coils on the blue radial convergence pole pieces.

Variable amplitude field-frequency waveforms from the hand-held unit are fed in at pin 2. After passing through voltage compensation diode D_2 the input signals control collector current in VT_2. Current from the blue static convergence control slider may flow in either direction through R_{11} in VT_2 collector circuit. Collector current from VT_2 can thus either add to or subtract from this current, imparting a field rate variation as required. This modulated shift current passes through the large coils on the blue radial pole pieces as described in Section 9b.

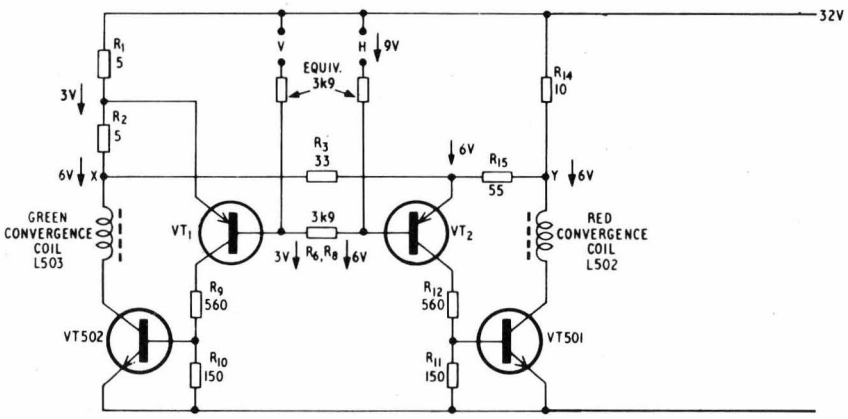


Fig. 9.5

The complete active blue drive circuit, with the exception of power transistor VT503 and the convergence windings, is incorporated into a single thick-film assembly TF502. Zener diodes used for stabilising the bias supplies and associated dropping resistors are discrete components common to the RG and B circuits as shown.

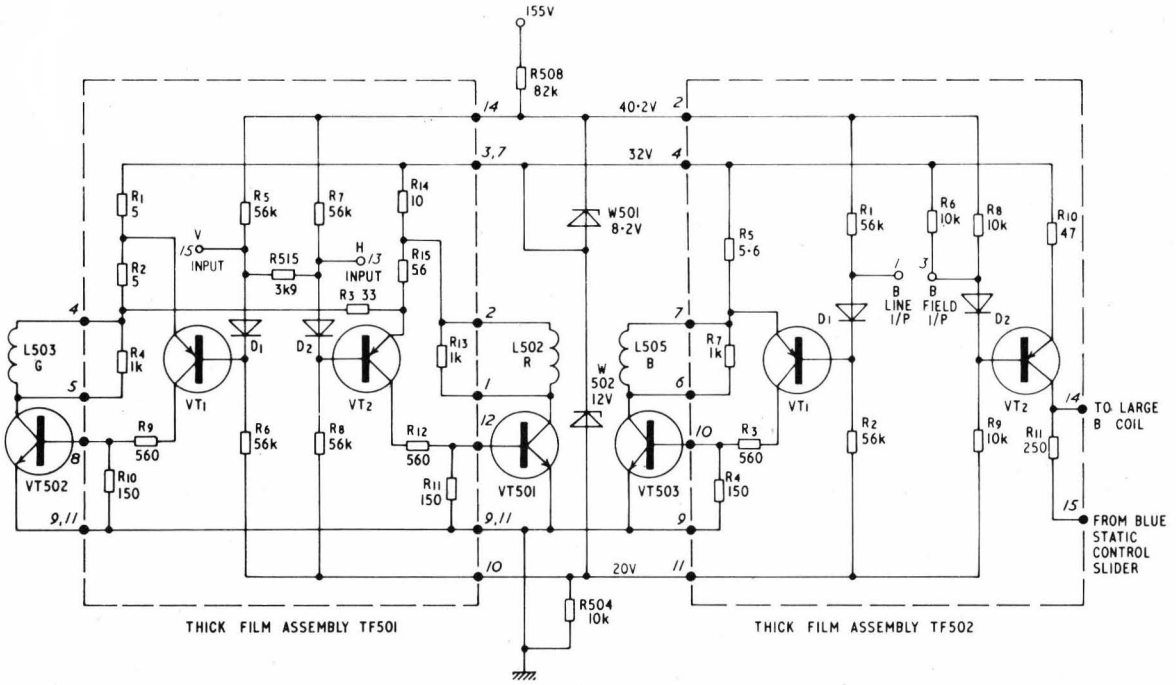


Fig. 9.6

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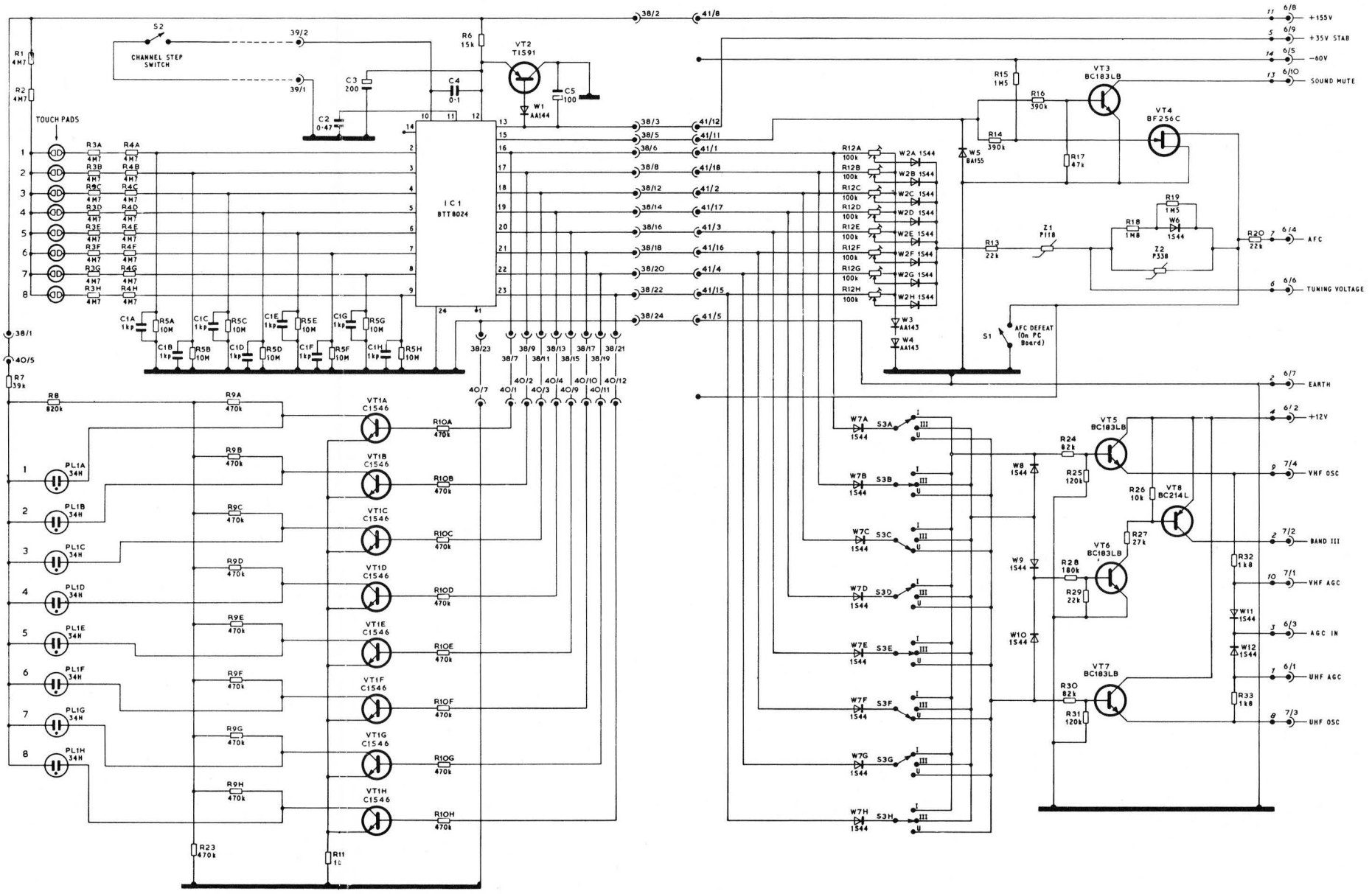
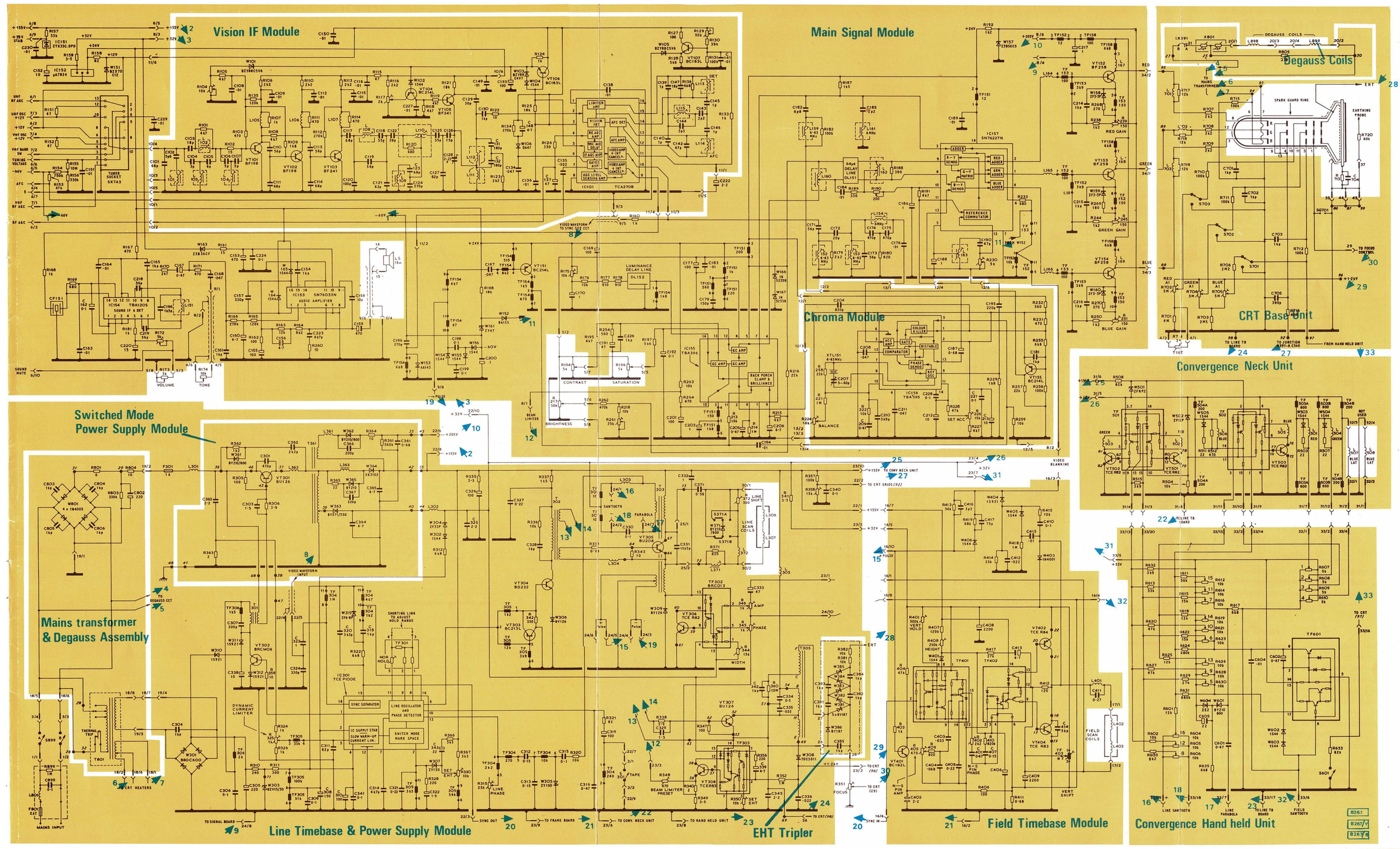

CHANNEL STEP SWITCH
TOUCH PADS
IC1 BTT8024
VT2 T1591
VT3 BC183LB
VT4 BF256C
VT5 BC183LB
VT6 BC183LB
VT7 BC183LB
VT8 BC214L
VT1A C1546
+155V
+35V STAB
-60V
SOUND MUTE
AFC
TUNING VOLTAGE
AFC DEFEAT (On PC Board)
EARTH
+12V
VHF OSC
BAND III
VHF AGC
AGC IN
UHF AGC
UHF OSC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