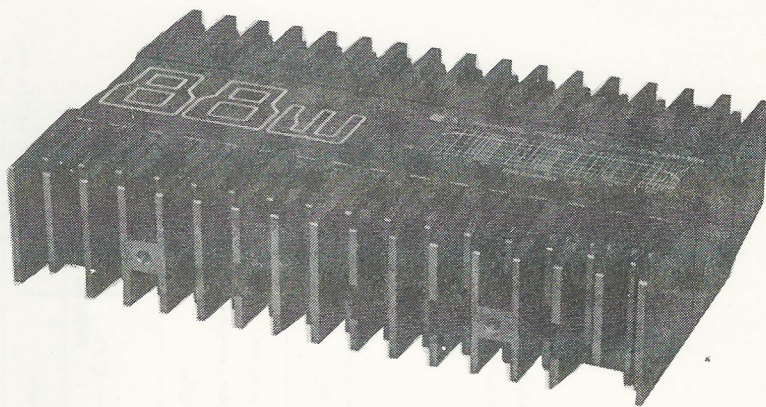


Service
Service
Service



Service Manual

12 V 

SPECIFICATIONS

INPUT VOLTAGE	100 mV
INPUT IMPEDANCE	9k OHMS (4 CHANNELS)
POWER OUTPUT	12 WATTS PER CHANNEL (APPROXIMATE)
SPEAKER IMPEDANCE	4 OHMS PER CHANNEL
POWER INPUT	12 VOLTS, NEGATIVE TO EARTH
CURRENT	8 AMPS (MAXIMUM)
SEMI-CONDUCTORS	4 I.C.s 2 DIODES

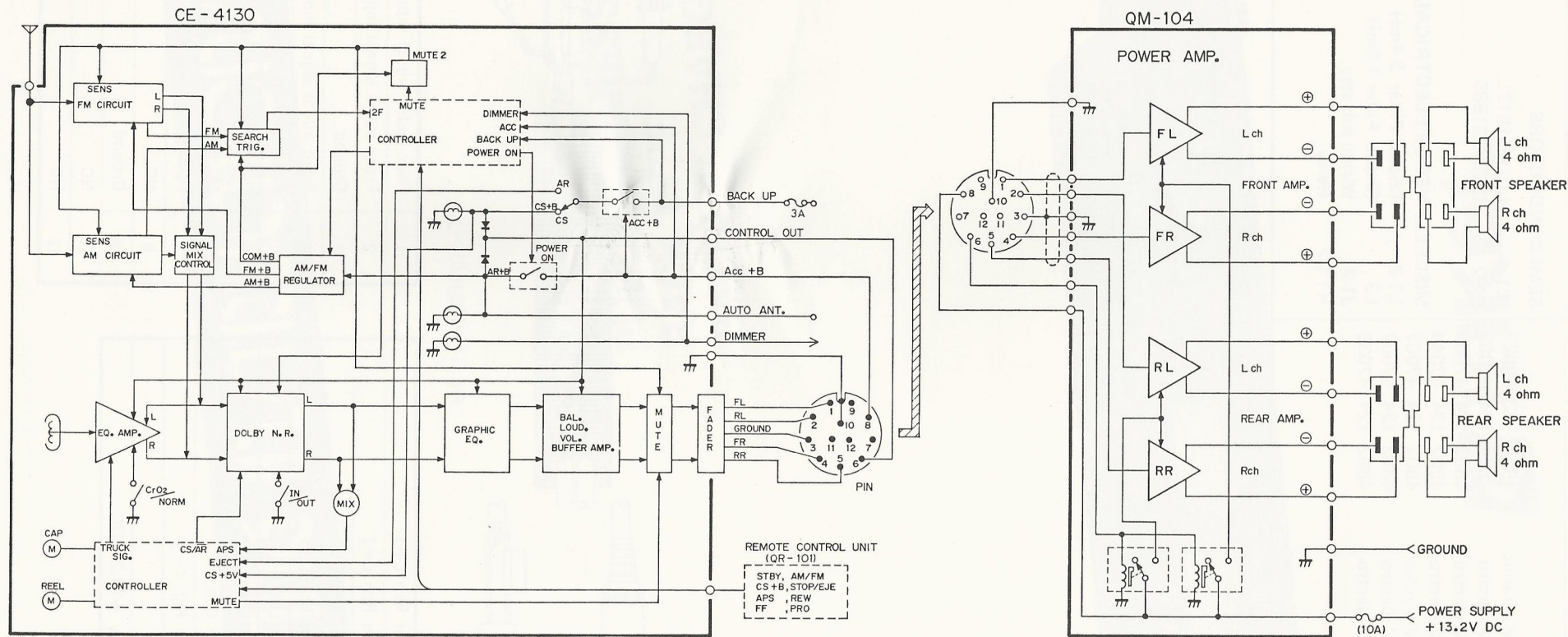
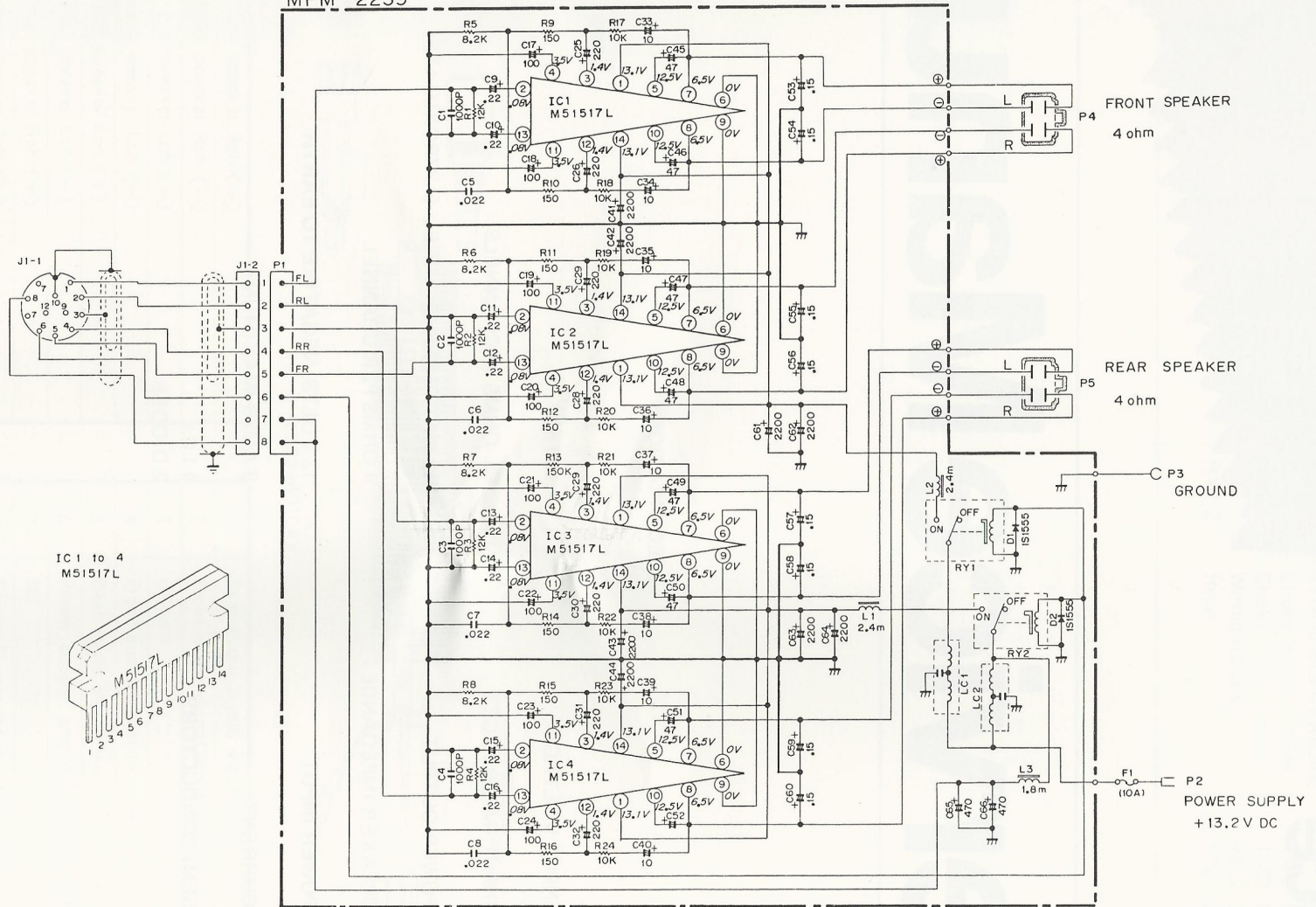


Fig. 2 (C32440104)



NOTES: 1. All capacitance in farad, $\mu=10^{-6}$, P= 10^{-12}

2. All resistance in ohm, K= 10^3 , M= 10^6

3. All inductance in henry, m= 10^{-3} , $\mu=10^{-6}$

4. DC voltages against the chassis measured with 100k ohm/volt meter, power supply set at +13.2 VDC no signal input.

Fig. 3 (C24440104)

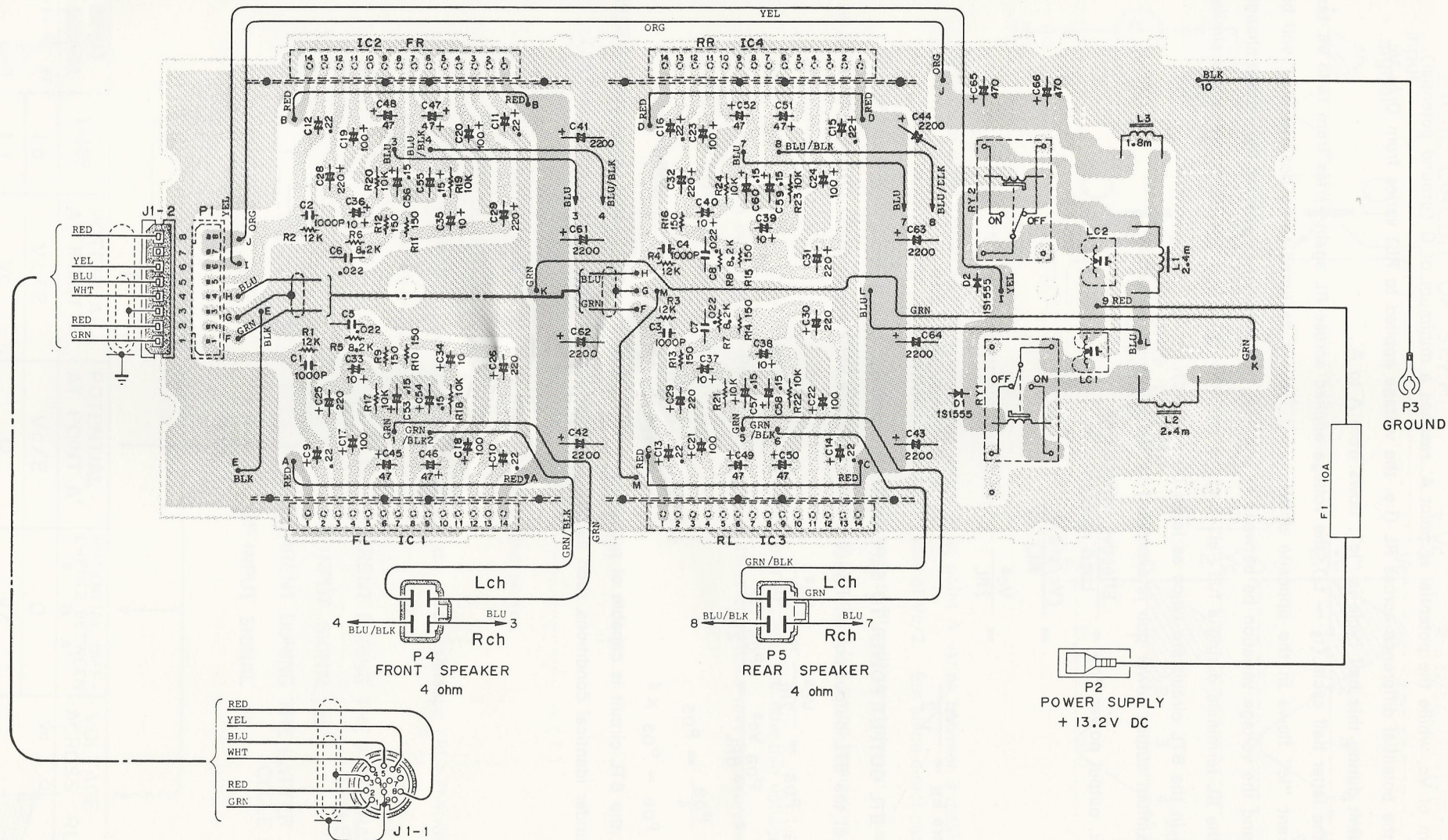


Fig. 4 (C27440104)

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
IC														
IC 1 to 4	13.1	.08	1.4	3.5	12.5	0	6.5	6.5	0	12.5	3.5	1.4	.08	13.1

(Unit: V)

THE BTL CIRCUIT SYSTEM

1. OPERATING PRINCIPLE

The basic circuit diagram of a BTL circuit is shown in Fig. 6 (with resistors and capacitors omitted). Both AMP 1 and AMP 2 are composed of identical SEPP circuits. The 4 transistors are arranged to form a Wheatstone bridge, with a load resistance (R_L) connected between the output terminals (A-A') of both amplifier circuits. An important feature in the QM-104 is the phase inverter circuit inserted in the circuit for AMP 2.

When an input signal "ei" is applied to the input terminals, it is applied unchanged to the AMP 1 input, but is first inverted by 180° (i.e. becomes "-ei") before being applied to AMP 2.

Consequently, during a full swing of the first half of the cycle (shaded portion), the potential at point A (AMP 1) will increase to the maximum V_c (voltage of power source) via Q1 (collector-emitter) (Q2 is turned OFF), but the potential at point A' (AMP 2) will decrease to a minimum of 0V (ground potential) via Q4 (collector-emitter) (Q3 is turned OFF). Therefore, the potential difference between the two ends of R_L will be the sum of the 2 voltage changes applied to A and A'.

The output current "ic" flowing during this period from $+V_c \rightarrow Q1$ (collector) $\rightarrow Q1$ (emitter) $\rightarrow R_L \rightarrow Q4$ (emitter) $\rightarrow Q4$ (collector) $\rightarrow 0$ (ground).

In the same manner, Q2 and Q3 are turned ON, and Q1 and Q4 turned OFF during the latter half of the ei cycle.

The output current "ic" then flows from $+V_c \rightarrow Q3$ (collector) $\rightarrow Q3$ (emitter) $\rightarrow R_L \rightarrow Q2$ (emitter) $\rightarrow Q2$ (collector) $\rightarrow 0$ (ground).

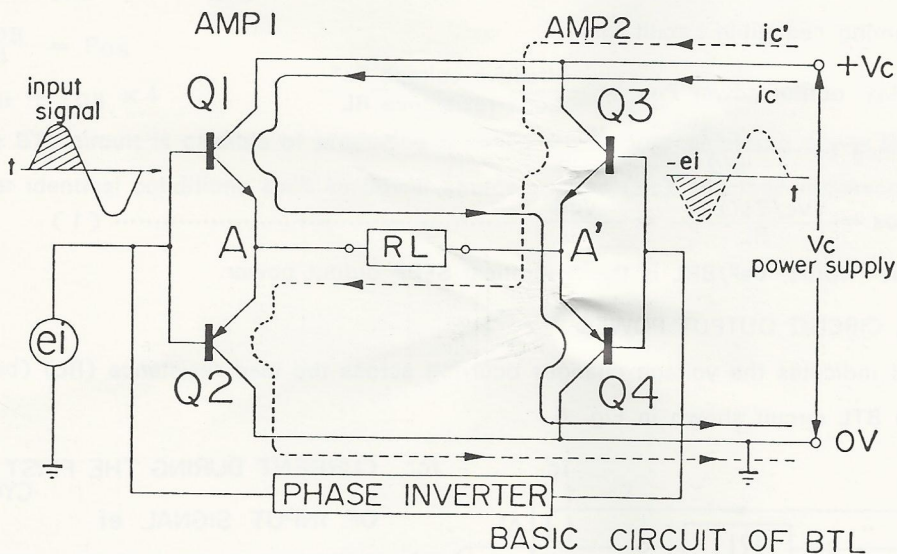


Fig. 6

2. COMPARISON BETWEEN SEPP AND BTL CIRCUITS

2-1. SEPP CIRCUIT OUTPUT POWER

Fig. 7 shows how a single SEPP circuit (for example, AMP 1 in Fig. 6 above) operates.

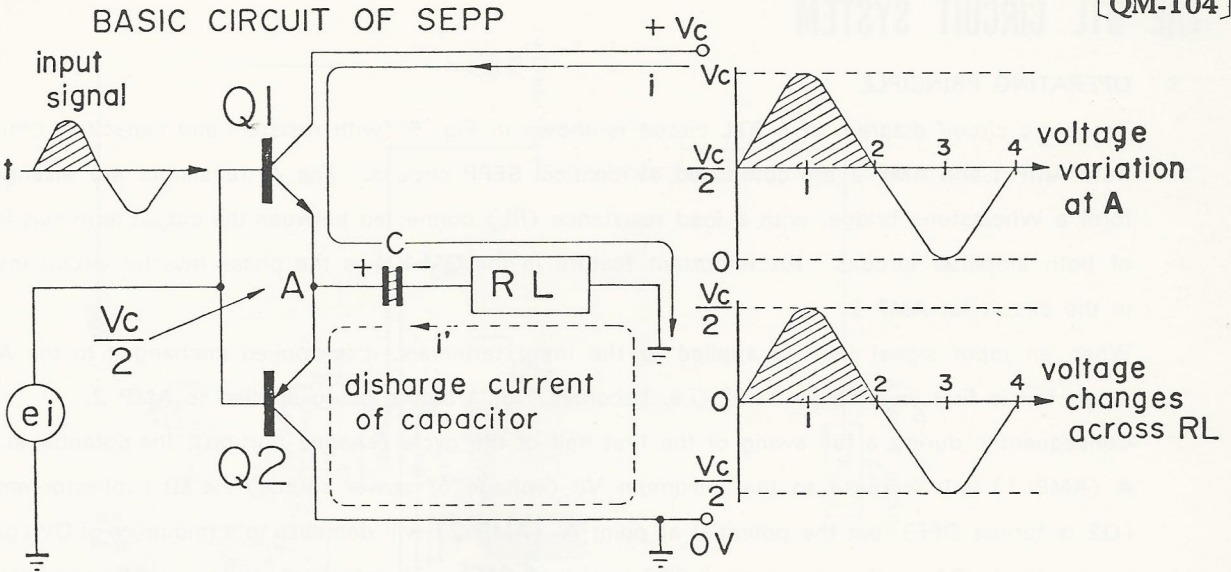


Fig. 7

When the input signal "ei" is applied, the potential at point A varies between a maximum of V_c and a minimum of 0 (ground potential) with a central value of $V_c/2$. But since direct current is blocked by capacitor C, the potential difference across both ends of R_L will vary between a maximum of $V_c/2$ and a minimum of $-V_c/2$, centering around 0. (This is assuming full swing transistors, and negligible circuit loss).

Since output power is determined by the load resistance R_L , and the effective voltage E_s applied to R_L , the maximum output power P_{os} available under these conditions may be expressed as follows: (Assuming negligible circuit loss)

$$\text{Max. output power } P_{os} = \frac{\text{Effective voltage } E_s^2}{\text{Load resistance } R_L}$$

$$\text{Since } E_s = \frac{V_c/2}{\sqrt{2}} = \frac{V_c}{2\sqrt{2}}$$

$$P_{os} = \frac{(V_c/2\sqrt{2})^2}{R_L} = \frac{V_c^2}{8R_L} \dots \dots \dots (1)$$

In other words, $V_s^2/8R_L$ is the theoretical SEPP output power.

2-2 BTL CIRCUIT OUTPUT POWER

Fig. 8 indicates the voltage changes occurring across the load resistance (R_L) (between A and A') in the BTL circuit shown in Fig. 6.

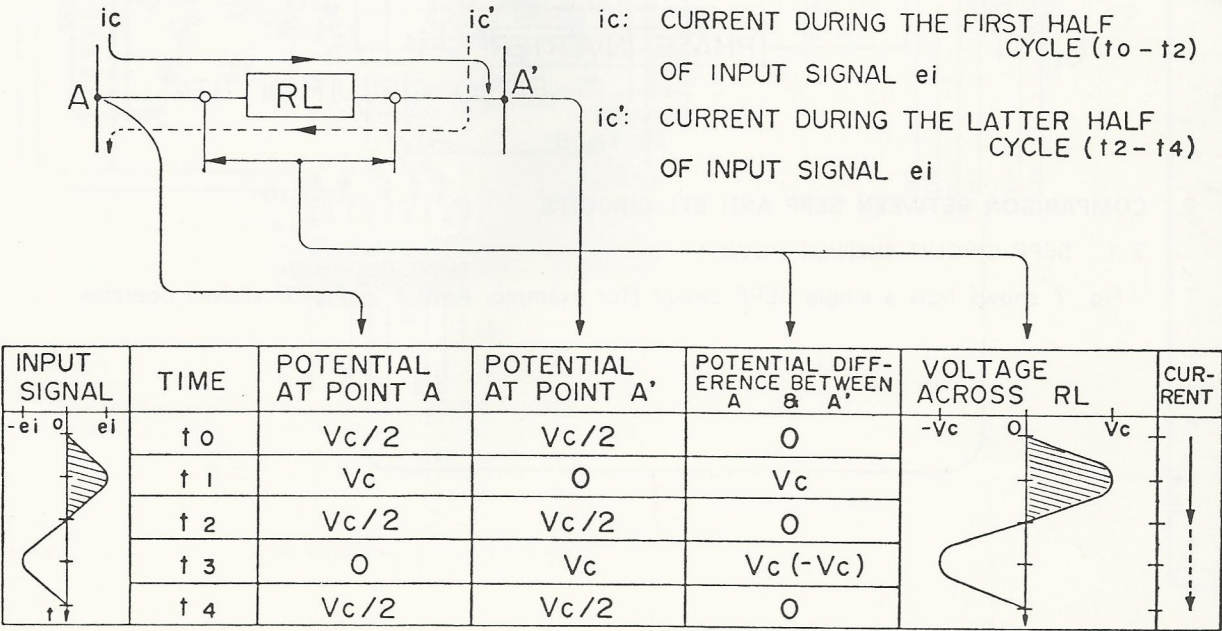


Fig. 8

During the first half cycle ($t_0 \sim t_2$) of the input signal "ei", the potential at point A reaches a maximum of V_c , while the potential at point A' reaches a minimum of 0 (ground potential).

Hence, the potential difference across R_L (i.e. the voltage applied to R_L) varies from 0 to V_c .

The current during this half cycle is "ic", flows from A to A'.

During the latter half cycle ($t_2 \sim t_4$), the voltage applied across R_L again varies from 0 to V_c , but the current "ic" flows in the opposite direction. If "ic" is assumed to be positive, "ic" will be minus, and the voltage variation be between 0 and $-V_c$. Consequently, whereas the voltage change across the R_L terminals during a full "ei" cycle is only $0 \sim \pm V_c/2$ in the SEPP circuit, the similar changes in the BTL circuit are twice as large ($0 \sim \pm V_c$).

The maximum output power P_{OB} is expressed by the following formula :-

$$\begin{aligned} \text{Max. output power } P_{OB} &= \frac{\text{Effective voltage } E_B^2}{\text{Load resistance } R_L} \\ &= \frac{(V_c/\sqrt{2})^2}{R_L} \\ &= \frac{V_c^2}{2R_L} \dots\dots\dots (2) \end{aligned}$$

$$\text{where } E_B = \frac{V_c}{\sqrt{2}}$$

3. RATIO OF BTL OUTPUT POWER TO SEPP OUTPUT POWER

The ratio of the BTL output power, P_{OB} (equation 2) to the SEPP output power, P_{OS} (equation 1) is :-

$$P_{OB} : P_{OS} = \frac{V_c^2}{2R_L} = \frac{V_c^2}{8R_L}$$

$$\text{i. e. } \frac{P_{OB} V_c^2}{8R_L} = \frac{P_{OS} V_c^2}{2R_L}$$

$$* \frac{P_{OB}}{4} = P_{OS}$$

$$* P_{OB} = P_{OS} \times 4$$

That is, the BTL circuit is capable of producing 4 times the amount of output power than the SEPP circuit under identical conditions such as power source voltage (V_c) and load resistance (R_L).